Design Example Report

Title	***60 W Isolated Flyback Power Supply Using 900 V InnoSwitch™3-EP PowiGaN™ INN3699C-H606***
Specification	90 VAC – 420 VAC Input; 12 V / 5 A Output
Application	Industrial Application
Author	Applications Engineering Department
Document Number	DER-982
Date	April 10, 2024
Revision	1.0

Summary and Features

- Off-line CV/CC QR flyback integrated switcher IC with 900 V PowiGaN and synchronous rectification for higher efficiency
- < 120 mW no-load input power up to 420 VAC
    - < 70 mW at 230 VAC
- Very high average efficiency
    - >92 % at 115 VAC and 230 VAC
    - >90 % from 90 VAC up to 420 VAC
- Very high full-load efficiency
    - >92 % at 115 VAC and 230 VAC
- No optocoupler increases reliability
- Meets EN550022 and CISPR-22 Class B conducted EMI with ≥ 6db margin
- Very low component count: 68 components

PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a 12 V / 5 A power supply using the InnoSwitch™3-EP 900 V PowiGaN™ INN3699C-H606 IC. This design shows a high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-EP controller and PowiGaN providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

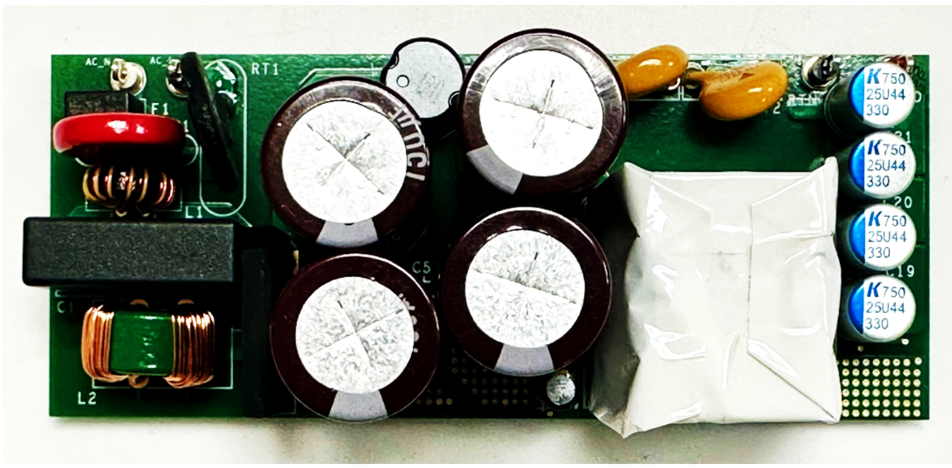


Figure 1 – Populated Circuit Board Photograph, Top.

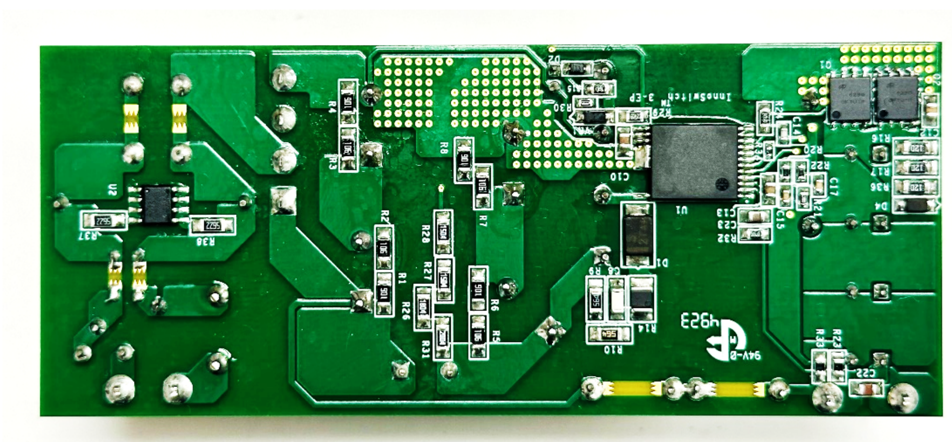


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the result section.

Description	Symbol	Min	Nom	Max	Units	Comment
Input						
Voltage	V_{IN}	90	115/230	420	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				<120	mW	Vin: 90 VAC – 420 VAC
Output						
Output Voltage	V_{OUT}	11.4	12	12.6	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			120	mV	20 MHz Bandwidth, at 25 Deg°C Ambient
Output Current	I_{OUT}		5		A	
Total Output Power						
Continuous Output Power	P_{OUT}		60		W	
Efficiency	η		91			Average @ 90 VAC
			92			Average @ 115 VAC
			92			Average @ 230 VAC
			92			Average @ 265 VAC
			91			Average @ 420 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge (Differential)				6	kV	1.2/50 μs Surge, IEC 61000-4-5, Impedance: 2 Ω Class A
Combination Wave Surge Test				6	kV	
EFT				4	kV	IEC 61000-4-4
ESD – Air Discharge				±16.5	kV	
ESD – Contact Discharge				±8.8	kV	
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

3 Schematic

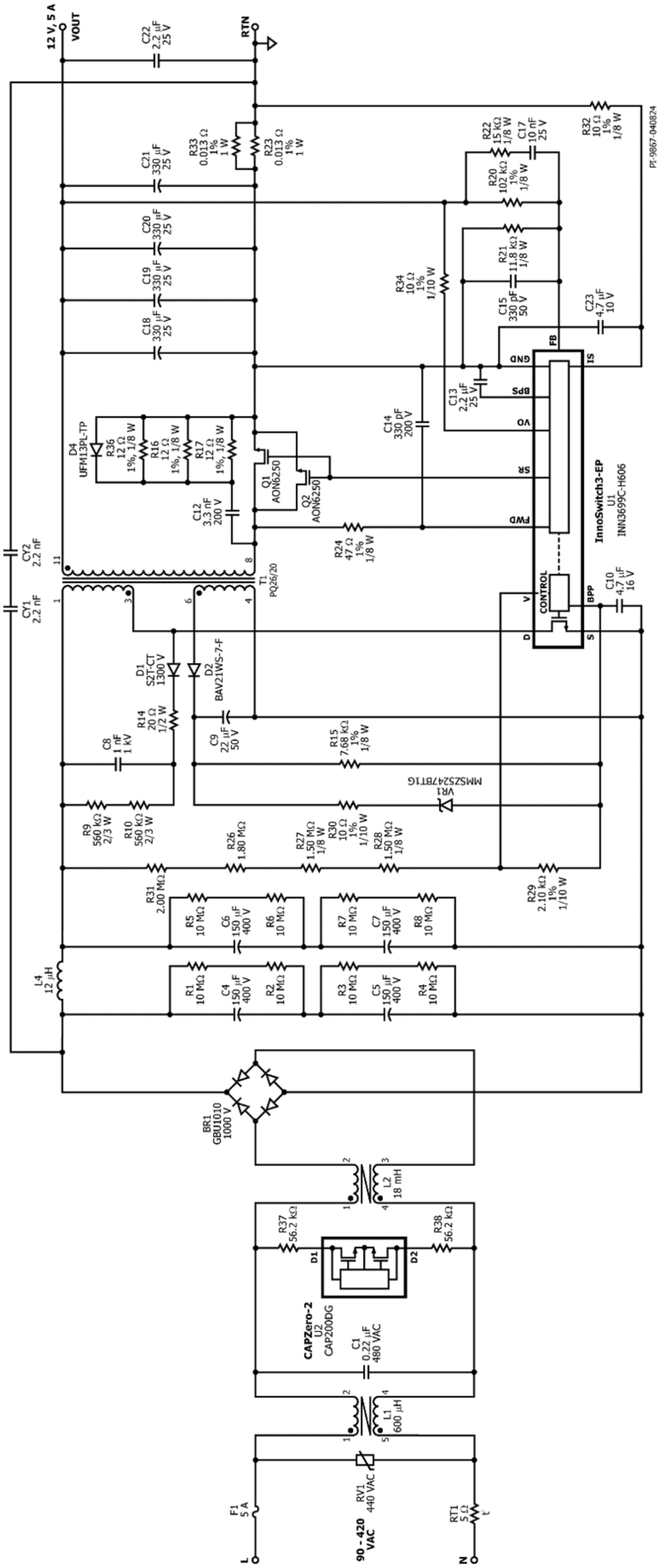


Figure 3 – Power Stage Schematic.

4 Circuit Description

The InnoSwitch3-EP combines primary, secondary and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates 900 V PowiGaN primary switch, primary-side controller, secondary-side controller for synchronous rectification and FluxLink™ technology that eliminates the need for an optocoupler needed on a secondary sensed feedback system. The InnoSwitch3-EP IC operates in quasi-resonant to achieve high efficiency.

4.1 Input EMI Filtering and AC Rectifier Stage

Fuse F1 isolates the circuit and provides protection from component failure while RT1 reduces inrush current. Varistor VR1 clamps input voltage spike from input surge voltage. X capacitor C1 and common mode chokes L1 and L2 forms a filter to attenuate common mode noise. Voltage across C1 is discharged by CAPZero™-2 IC U2, R37 and R38 to meet safety discharge time requirement duration in absence of input voltage. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the input filter capacitor C4, C5, C6 and C7. Common mode choke L4 connected in between input filter capacitors form input pi-filter. It attenuates both common and differential mode noise. Capacitors CY1 and CY2 are used to mitigate the common mode EMI. Resistors R1, R2, R3, R4, R5, R6, R7 and R8 are used to evenly balance the voltage across input filter capacitors.

4.2 InnoSwitch3-EP IC Primary

One end of the transformer (T1) primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch3-EP IC (U1). Resistors R26, R27, R28, R29 and R31 provide input voltage sense protection for over and undervoltage conditions.

A low-cost RCD clamp formed by diode D1, resistors R14, R9, R10 and capacitor C8 limits the peak drain voltage of U1 at turn-off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C10) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C9. Resistor R15 limits the current being supplied to the BPP pin of the InnoSwitch3-EP IC (U1).

Zener diode VR1 in series with R30 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1 which then causes a current to flow into the BPP pin of InnoSwitch3-EP IC U1. If the current flowing into the BPP pin increases above the

I_{SD} threshold, the InnoSwitch3-EP controller will undergo auto restart to protect itself from any damage.

4.3 InnoSwitch3-EP IC Secondary

The secondary-side of the InnoSwitch3-EP IC provides output voltage, output current sensing and drive to the SR FET providing synchronous rectification. The secondary of the transformer is rectified by SR FET Q1, Q2 and filtered by output capacitors C18, C19, C20, C21 and C22. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via an RCD snubber R16, R17, R36, C12 and D4. Diode D4 is used to minimize power dissipation in resistors R16, R17 and R36.

The gates of Q1 and Q2 are turned on by secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R24 and fed into the FWD pin of the IC. The FWD pin is also used to supply the secondary-side of IC U1 when the VOUT pin is below threshold value. Capacitor C14 prevents high voltage spike on the FWD pin.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C13 connected to the BPS pin of InnoSwitch3-EP IC U1 provides decoupling for the internal circuitry.

Output current is sensed by monitoring the voltage drop across resistor R23 and R33 between the IS and GND pins with a threshold of approximately 36 mV to reduce losses. Capacitor C23 and resistor R32 provide filtering on the IS pin from external noise.

The device operates in constant voltage mode before reaching the current limit. During constant voltage mode operation, output voltage regulation is achieved through sensing the output voltage via divider resistors R20 and R21. The voltage across R17 is fed into the FB pin with an internal reference voltage threshold of 1.265 V. Output voltage is regulated to achieve a voltage of 1.265 V on the FB pin. Capacitor C15 provides decoupling from high frequency noise affecting FB pin, while C17 and R22 is the feedforward network to speed up the response time to lower the output ripple. Resistor R34 in series with the VO pin acts as protection when common mode surge and ESD is injected in the output pins.

5 PCB Layout

PCB copper thickness is 2.0 oz.
PCB Material Thickness is 0.062 inches.
PCB Material is FR4.

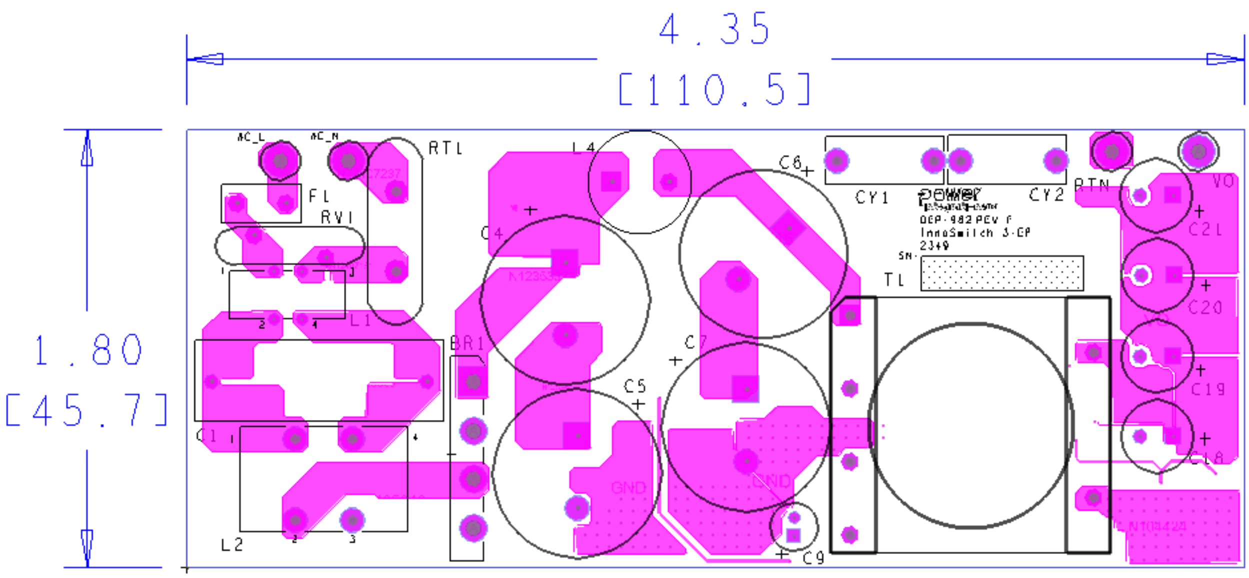


Figure 4 – Printed Circuit Layout, Top.

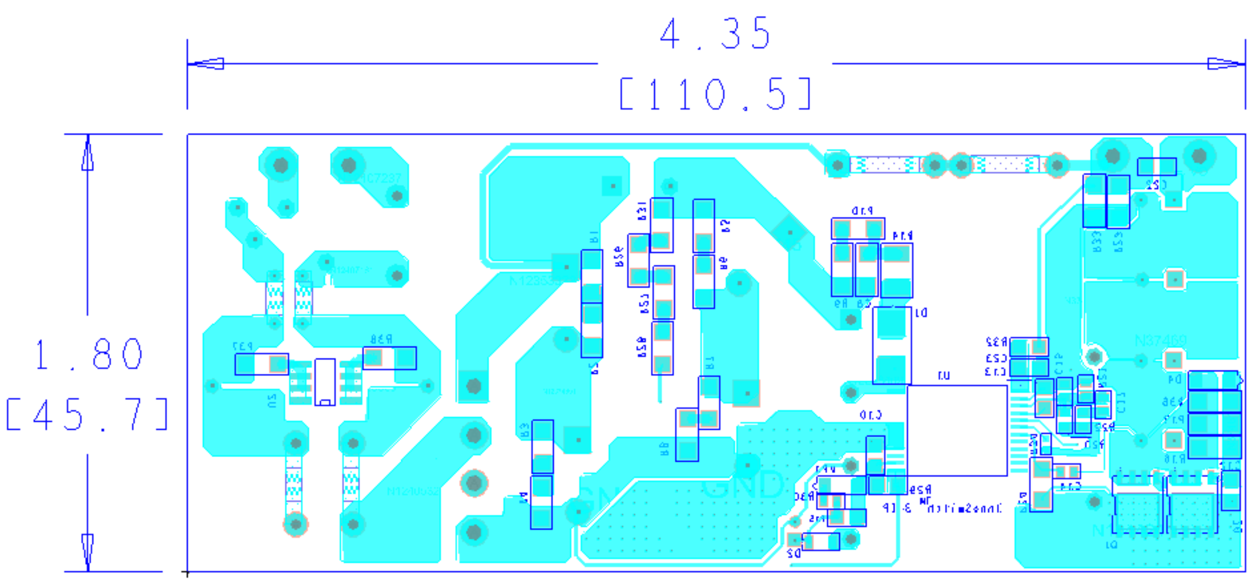


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

6.1 Bill of Material: Electrical Components

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	Bridge Rectifier, Single Phase, Standard, 1 kV, Through Hole GBU	GBU1010	SMC Diode
2	1	C1	0.22 μF, ±20%, Film Capacitor 480 V 1 kV Polypropylene (PP), Metallized Radial, 26 mmL x 8.5 mmW x 18 mmH x 22.5 mmLS	F339X142248MIP2T0	Vishay
3	4	C4 C5 C6 C7	150 μF, ±20%, 400 V, Electrolytic, (18 x 31.5)	EKWB401ELL151MMN3S	United Chemi-Con
4	1	C8	1000 pF, ±10%, 1000V (1kV), Ceramic Capacitor, C0G, NP0 1206	C1206C102KDGACAUTO	Kemet
5	1	C9	22 μF, 50 V, Aluminum Electrolytic Capacitors, Radial, Can 2000 Hrs @ 85°C, (5 x 11), LS 2 mm	EEU-FM1H220H	Panasonic
6	1	C10	4.7 μF, 16 V, Ceramic, X7R, 0805	CL21B475KOFNNNE	Samsung
7	1	C12	3.3 nF, 200 V, Ceramic, X7R, 0805	08052C332KAT2A	AVX
8	1	C13	2.2 μF, ±10%, 25 V, Ceramic Capacitor X7R, 0805	CL21B225KAFNFNE	Samsung
9	1	C14	330 pF ±5% 250 V Ceramic Capacitor C0G, NP0 0603	CGA3E3C0G2E331J080AA	TDK
10	1	C15	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
11	1	C17	10 nF, 0.01 μF, ±10%, 25 V, Ceramic Capacitor, X7R, General Purpose, -55 °C ~ 125 °C, 0603	CL10B103KA8NFNC	Samsung
12	4	C18 C19 C20 C21	330 μF, ±20%, 25 V, Al Organic Polymer, Gen. Purpose, Can, 18 mΩ, 2000 Hrs @ 105°C, (8 mm x 13 mm	A750KS337M1EAAE018	KEMET
13	1	C22	2.2 μF, ±10%, 25 V, X7R, r, -55°C ~ 125°C, 0805	CL21B225KAFVPNE	Samsung
14	1	C23	4.7 μF ±10% 10V Ceramic Capacitor X7R 0805	LMK212B7475KGHT	Taiyo Yuden
15	2	CY1 CY2	CAP, 2200 pF, ±20% ,760 VAC, Ceramic Capacitor Y5U (E) Radial, Disc	AY1222M47Y5UC63L0	Vishay
16	1	D1	Diode, Standard, 1300 V, 2 A, SMT SMB, (DO-214AA)	S2T-CT	Diotec Semi
17	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
18	1	D4	Diode, GEN PURP, 200V, 1A, SOD-123F, SOD123FL	UFM13PL-TP	Micro Commercial
19	1	F1	5 A, 250 V, Slow, Long Time Lag, RST	RST 5	Belfuse
20	1	L1	600 μH, Toroidal CMC, custom, DER-536, wound on 32-00275-00 core, Added FP for DER601 lkn110117.	32-00347-00	Power Integrations
21	1	L2	Custom, CMC, 18 mH @ 10 kHz, Toroidal, 17.5 mm OD x 11.0 mm thick. 40 turns x 2, 0.40 mm wire 190 mΩ max	04291-T231	Sumida
22	1	L4	Fixed Inductor, 12 μH @100 kHz, ± 10%, 5.1 A, 0.035ohm, AEC-Q200, Unshielded, Ferrite, Radial, -40°C ~ 85°C, 11 x 11.5 mm	RFB1010-120L	Coilcraft
23	2	Q1 Q2	MOSFET, N-CH, 150 V, 52 A, 8DFN	AON6250	Alpha & Omega Semi
24	8	R1 R2 R3 R4 R5 R6 R7 R8	RES, 10 MΩ, 5%, 1/4 W, Thick Film, 1206	RC1206FR-0710ML	YAGEO
25	2	R9 R10	RES, 560 kΩ, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J564V	Panasonic
26	1	R14	RES, 20 Ω, ±5%, 1/2W, 1210, Thick Film	CRCW121020R0JNEA	Vishay
27	1	R15	RES, 7.68 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF7681V	Panasonic
28	3	R16 R17 R36	RES, 12 Ω, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J120V	Panasonic
29	1	R20	RES, 102 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1023V	Panasonic
30	1	R21	RES, 11.8 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1182V	Panasonic
31	1	R22	RES, 15 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1502V	Panasonic
32	2	R23 R33	RES,13 mΩ ±1% 1W Chip Resistor 1206 Automotive AEC-Q200, Current Sense Thick Film	ERJ-8BWFR013V	Panasonic
33	1	R24	RES, 47.0 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF47R0V	Panasonic
34	1	R26	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic

35	2	R27 R28	RES, 1.50 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1504V	Panasonic
36	1	R29	RES, 210 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2103V	Panasonic
37	1	R30	RES, 10 Ω, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
38	1	R31	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
39	1	R32	RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
40	1	R34	RES, 10 Ω, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF10R0X	Panasonic
41	2	R37 R38	RES, 56.2 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF5622V	Panasonic
42	1	RT1	NTC Thermistor, 2.5 Ω, 8 A	CL-30	Thermometrics
43	1	RV1	715 V 6 kA Varistor 1 Circuit Through Hole Disc 14 mm	V14E440P	Littelfuse
44	1	T1	Bobbin, PQ26/20, Vertical, 12 pins	B65878E0012D001	TDK
45	1	U1	InnoSwitch3-EP Switch Integrated Circuit, 900 V, InSOP24D	INN3699C-H606	Power Integrations
46	1	U2	CAPZero-2, SO-8C	CAP200DG	Power Integrations
47	1	VR1	DIODE, ZENER, 17 V, ±5%, 500 mW, SOD123, SOD-123	MMSZ5247BT1G	ON Semi

6.2 Bill of Material: Mechanical Components

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	AC_L	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
2	2	AC_N RTN	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
3	1	VO	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone

7 Transformer (T1) Specification

7.1 Electrical Diagram

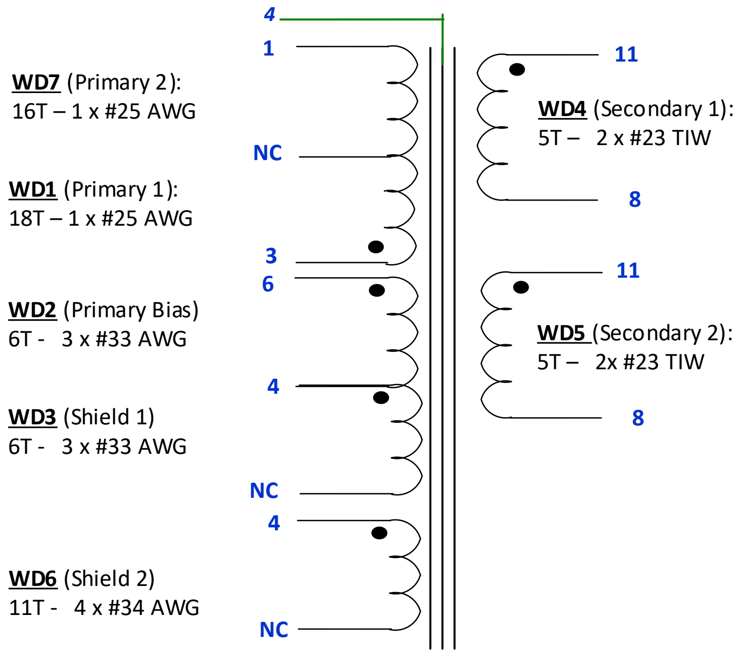


Figure 6 – Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, typical switching frequency, between pin 3 to pin 1, with all other windings open.	573 µH ±5.0%
Electrical Strength	60 Hz 1 second, from pins 1, 3, 4, 6 to pins 8, 9.	3000 VAC
Primary Leakage Inductance	Measured between pin 3 to pin 1, with all other windings shorted.	4.5 µH (Max.)

7.3 Materials List

Item	Description
[1]	Core: PQ2620, PC 95
[2]	Bobbin: PQ2620- V-12pins (25-01140-00).
[3]	Thin Copper Tape 0.5 mm.
[4]	Varnish; Dolph BC 359 or Equivalent.
[5]	Single Core Wire: #25 AWG, insulation Heavy Build.
[6]	Separation Tape: Polyester Film [1 mil (25.4 Micrometers) Base T 9 mm Wide.
[7]	Single Core Wire: #33 AWG (0.21 mm), Insulation Heavy Build.
[8]	Triple Insulated Wire: #23 AWG.
[9]	Single Core Wire: #34 AWG (0.19 mm), Insulation Heavy Build.
[10]	Separation Tape: 3M 1298 Polyester Film, 1 mil thick, 33.0 mm Wide.
[11]	Bus Wire: Uninsulated #26 AWG.

7.4 Transformer Build Diagram

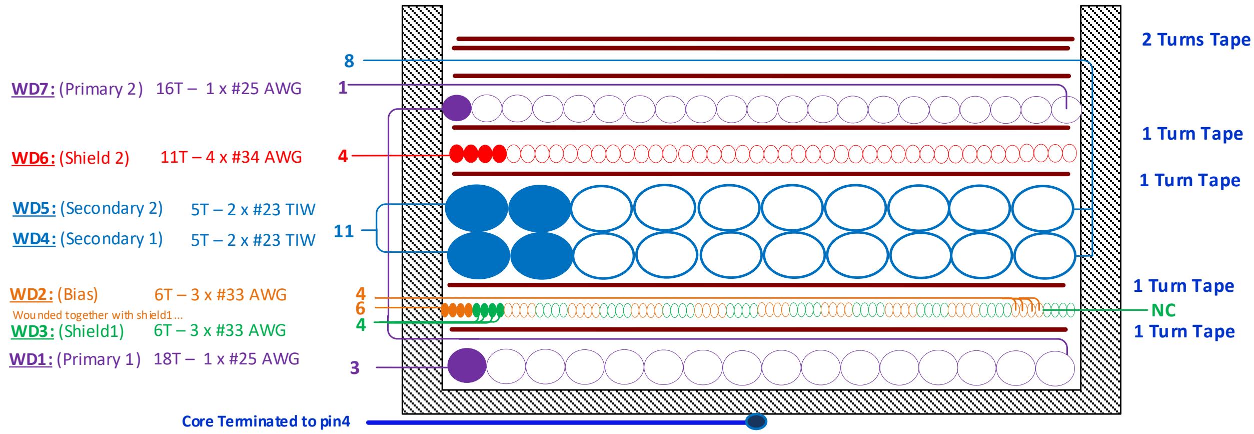
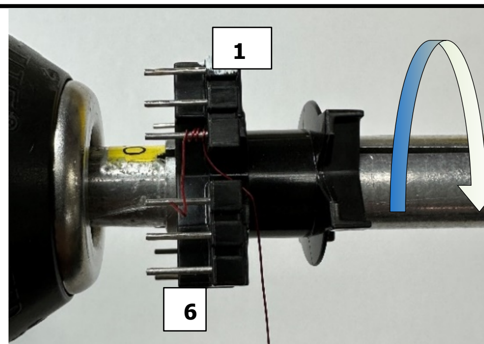
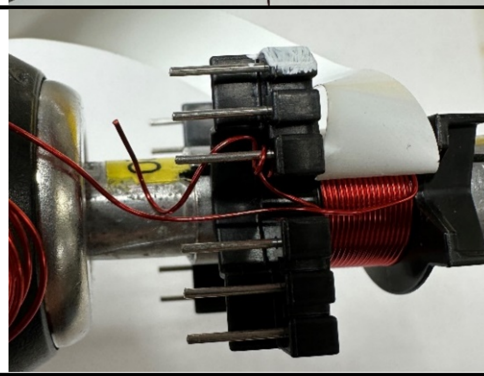
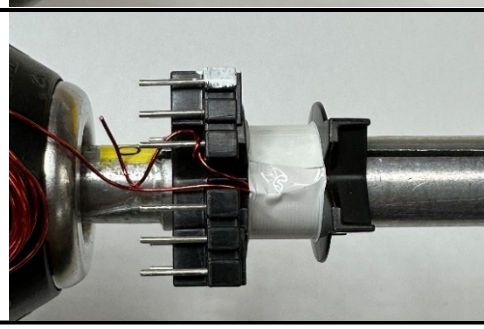
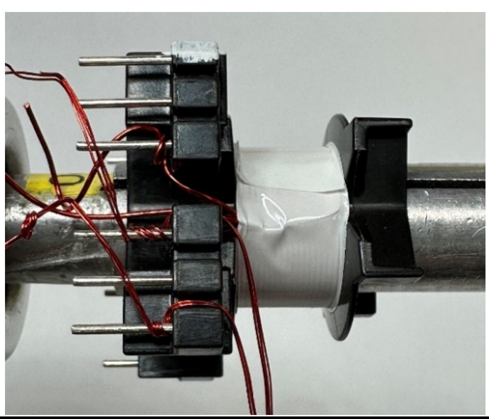


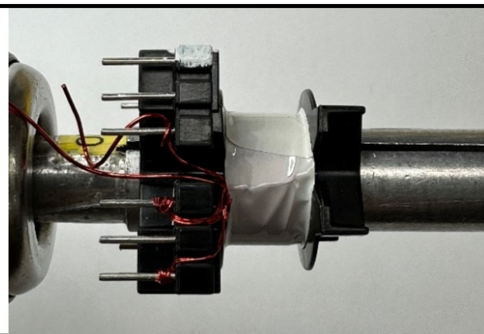
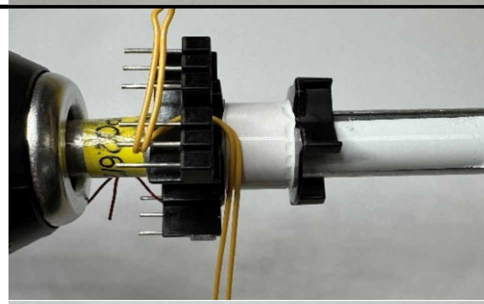
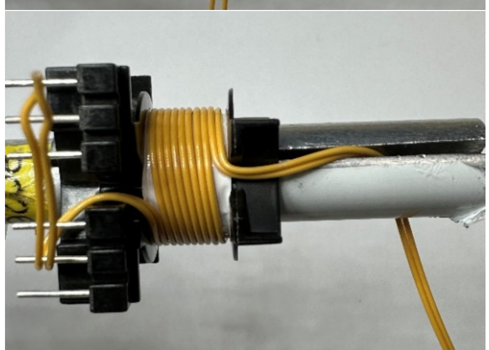
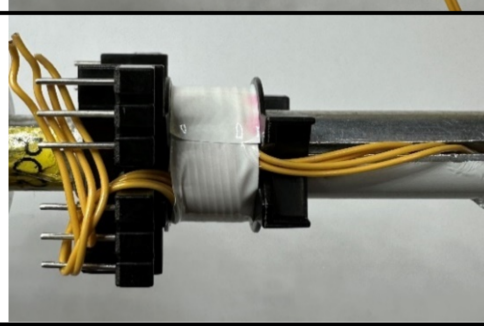
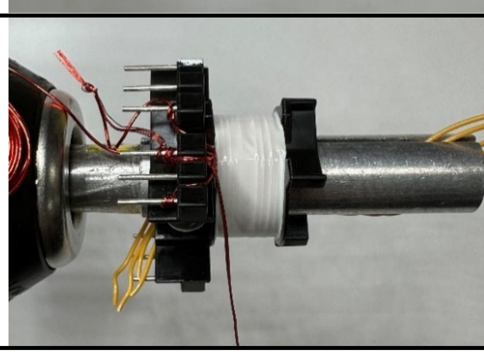
Figure 7 – Build Diagram.

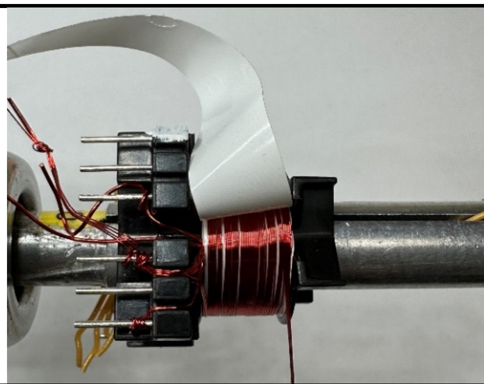
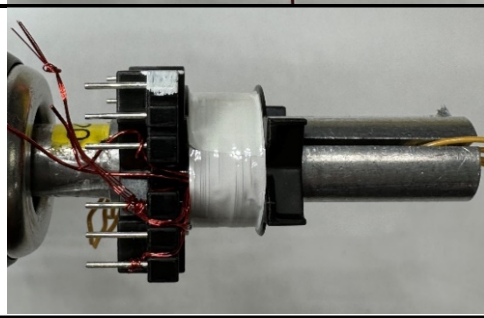
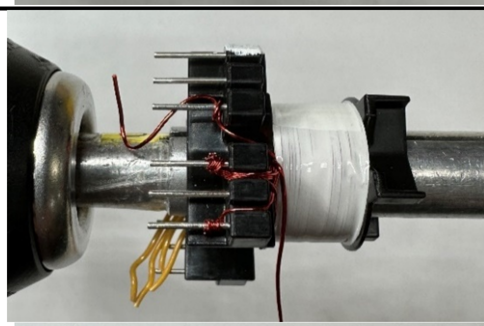
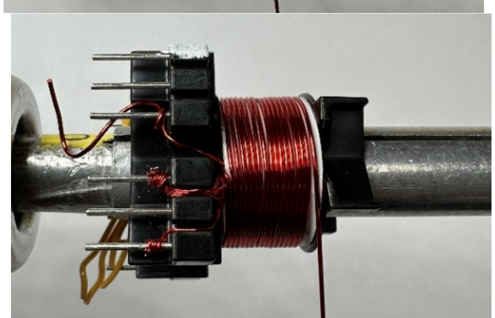
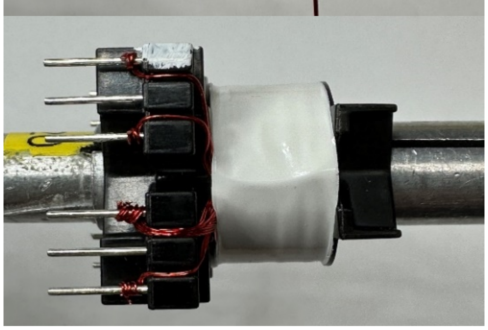
7.5 Transformer Instruction

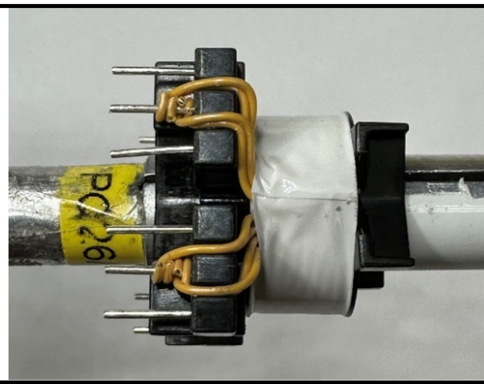
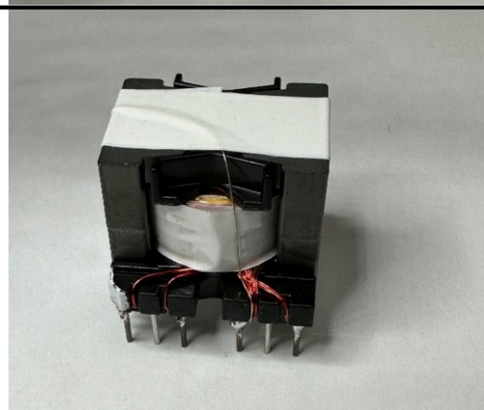
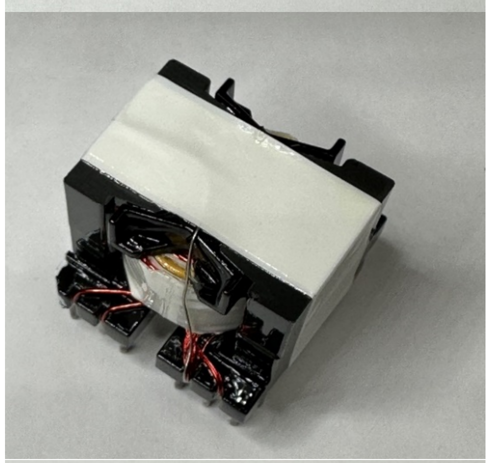
Winding Preparation	Position the bobbin Item [2] on the mandrel, pins facing the opposite direction of the winding machine, pin 1 on the lower side and pin 6 on the upper side. Winding direction is clockwise.
WD1: Primary 1	Start at pin 3, wind 18 turns of wire Item [5], from right to left in 1 layer. At the last turn, bring the wire where you started, and leave enough length of wire-floating for WD7-2nd Primary.
Insulation	1 layer of tape Item [6].
WD2: Bias & WD3: Shield1	Use 3 wires Item [7] start at pin 6 for Bias winding, also use 3 wires same Item [7] for WD3-Shield1 winding start at pin 3, winding right to left direction, wind all 8 wires in parallel for 6 turns, at the last turn terminate Bias winding at pin 4. For Shield1 winding cut the wire at the last turn, leave at least 3mm of excess to tuck it in the layer of tape.
Insulation	1 layer of tape Item [6].
WD4 & WD5: Secondary	Switch to the other side of bobbin, WD4 Start from pin 11 wind 2 wires of Item [8] for 5 turns, from left to right. Secure pin 8 with tape. Repeat the process 1 more time for WD5. WD5 wires winding should be on top of WD4.
Insulation	1 layer of tape Item [6].
WD6: Shield2	For WD6 Shield2 winding use 4 wires of Item [9] start at pin 4 from left to right. At the last turn cut and leave a floating wire with at least 3 mm, to tuck it in the layer of tape.
Insulation	1 layer of tape Item [6].
WD7: Primary 2	Use the floating wire from WD1-Primary 1, wind 8 turns from left to right to terminate the wire at pin 1.
Insulation	1 layer of tape Item [6].
Pin 8 Wire	Bring back 4 wires mark as pin 8 to the top of the bobbin terminate at pin 1.
Insulation	2 layers of tape Item [6] to secure all windings.
Finish	Gap Cores to get 573 μH. Solder a bus wire Item [11] then terminate at pin 4. Use 2 layers of tape Item [6] to secure the upper and lower part of the core. Remove pins: 2, 5,7, 9, 10, 12. Use 2 layers of tape Item [6] horizontally to secure the cores. Varnish Item [4] the transformer.

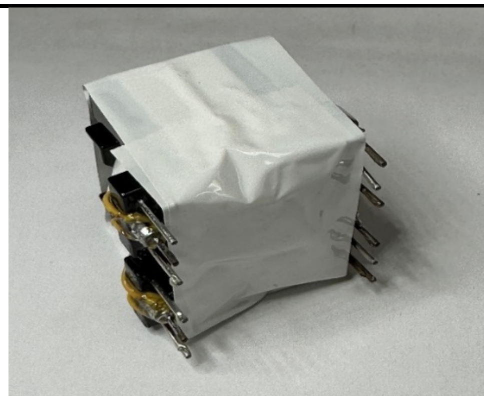
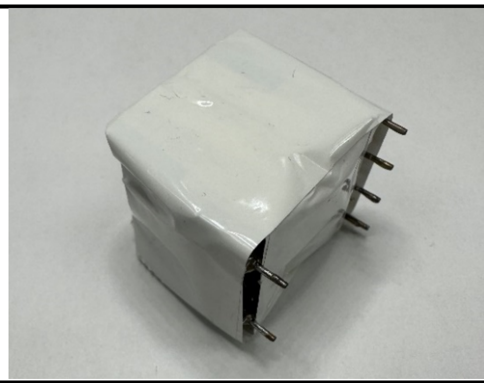
7.6 Winding Illustrations

Winding Preparation		Position the bobbin Item [2] on the mandrel, pins facing on the left side of the winding machine. Winding direction is clockwise.
WD1 Primary 1		Start at pin 3, wind 18 turns of wire Item [5], from left to right in 1 layer. At the last turn, bring the wire where you started, and leave enough length of wire-floating for WD7-2nd Primary.
Insulation		1 layer of tape Item [6].
WD2: Bias & WD3: Shield1		Use 3 wires Item [7] start at pin 6 for Bias winding, also use 3 wires same Item [7] for WD3-Shield1 winding start at pin 4, winding left to right direction, wind all 6 wires in parallel for 8 turns, at the last turn terminate Bias winding at pin 4. For Shield1 winding cut the wire at the last turn, leave at least 3 mm of excess to tuck it in the layer of tape.

Insulation		1 layer of tape Item [6].
WD4 **&** **WD5** **Secondary**	 	Switch to the other side of bobbin, WD4 start from pin 11 wind 2 wires of Item [8] for 5 turns, from left to right, at the last turn exit the wires at right slot, also leaving 50 mm floating and mark as Pin 8. Repeat the process 1 more time for WD5. WD5 wires winding should be on top of WD4.
Insulation		1 layer of tape Item [6].
WD6 **Shield2**		For WD6 Shield2 winding use 4 wires of Item [9] start at Pin 4 from left to right. At the last turn cut and leave a floating wire with at least 3 mm, to tuck it in the layer of tape.

		
Insulation		1 layer of tape Item [6].
WD7 **Primary 2**	 	Use the floating wire from WD1-Primary 1, wind 8 turns from left to right. Terminate the wire at pin 1.
Insulation		1 layer of tape Item [6].

Pin 8 Wire		Bring 4 wires mark as pin 8 to the left and terminate at pin 8. Secure with 2 layer of tape Item [6].
Varnish	  	Gap Cores Item [1] to get 573 µH. Use 2 layers of tape Item [6] horizontally to secure the cores. Solder a bus wire Item [11] then terminate at pin 4. Varnish Item [4].

	 	Remove pins: 2, 5, 7, 9,10, 12. Use a wide tape Item [10] to envelop bottom and secondary side part of the bobbin.
Finished Transformer		

8 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-EP900V_Flyback_031323; Rev.1.5; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-EP 900V Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
4	VIN_MIN	90		90	V	Minimum AC input voltage
5	VIN_MAX			420	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		Range of AC input voltage
7	LINEFREQ			60	Hz	AC Input voltage frequency
8	CAP_INPUT	150.0		150.0	uF	Input capacitor
9	VOUT			12.00	V	Output voltage at the board
10	PERCENT_CDC			0		Cable drop compensation desired at full-load
11	IOUT	5.000		5.000	A	Output current
12	POUT			60.00	W	Output power
13	EFFICIENCY	0.88		0.88		AC-DC efficiency estimate at full-load given that the converter is switching at the valley of the rectified minimum input AC voltage
14	FACTOR_Z			0.60		Z-factor estimate
15	ENCLOSURE			OPEN FRAME		Power supply enclosure
19	**PRIMARY CONTROLLER SELECTION**					
20	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
21	DEVICE_GENERIC	INN36X9C		INN36X9C		Generic device code
22	DEVICE_CODE			INN3699C		Actual device code
23	POUT_MAX			75	W	Power capability of the device based on thermal performance
24	RDSON_100DEG			0.58	Ω	Primary switch on time drain resistance at 100 degC
25	ILIMIT_MIN			1.980	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			2.130	A	Typical current limit of the primary switch
27	ILIMIT_MAX			2.279	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			900	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.37	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW			702.6	V	Peak drain voltage on the primary switch during turn-off
34	**WORST CASE ELECTRICAL PARAMETERS**					
35	FSWITCHING_MAX	86000		86000	Hz	Maximum switching frequency at full-load and valley of the rectified minimum AC input voltage
36	VOR	75.0		75.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			101.16	V	Valley of the minimum input AC voltage at full-load
38	KP			0.46		Measure of continuous/discontinuous mode of operation
39	MODE_OPERATION			CCM		Mode of operation
40	DUTYCYCLE			0.427		Primary switch duty cycle
41	TIME_ON			10.62	us	Primary switch on-time
42	TIME_OFF			6.67	us	Primary switch off-time
43	LPRIMARY_MIN			544.2	uH	Minimum primary inductance
44	LPRIMARY_TYP			572.8	uH	Typical primary inductance
45	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
46	LPRIMARY_MAX			601.5	uH	Maximum primary inductance
48	**PRIMARY CURRENT**					
49	IPEAK_PRIMARY			2.140	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			1.046	A	Primary switch current pedestal

51	IAVG_PRIMARY			0.636	A	Primary switch average current
52	IRIPPLE_PRIMARY			1.298	A	Primary switch ripple current
53	IRMS_PRIMARY			1.004	A	Primary switch RMS current
55	**SECONDARY CURRENT**					
56	IPEAK_SECONDARY			13.265	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			6.486	A	Secondary winding current pedestal
58	IRMS_SECONDARY			7.215	A	Secondary winding RMS current
62	**TRANSFORMER CONSTRUCTION PARAMETERS**					
63	**CORE SELECTION**					
64	CORE	PQ26		PQ26		Core selection
65	CORE CODE			PQ26/20-3C95		Core code
66	AE			121.00	mm^2	Core cross sectional area
67	LE			45.00	mm	Core magnetic path length
68	AL			7020	nH/turns^2	Ungapped core effective inductance
69	VE			5470.0	mm^3	Core volume
70	BOBBIN			PQ26/20 - 2 (P6-S6)		Bobbin
71	AW			31.10	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
72	BW			9.00	mm	Bobbin width
73	BH			4.78	mm	Bobbin height
74	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75	**PRIMARY WINDING**					
76	NPRIMARY			31		Primary turns
77	BPEAK			3740	Gauss	Peak flux density
78	BMAX			3393	Gauss	Maximum flux density
79	BAC			1003	Gauss	AC flux density (0.5 x Peak to Peak)
80	ALG			596	nH/turns^2	Typical gapped core effective inductance
86	**SECONDARY WINDING**					
87	NSECONDARY			5		Secondary turns
89	**BIAS WINDING**					
90	NBIAS			6		Bias turns
94	**PRIMARY COMPONENTS SELECTION**					
100	**LINE UNDERVOLTAGE**					
101	BROWN-IN REQURED			81.0	V	Required AC RMS line voltage brown-in threshold
102	RLS			6.32	MΩ	Connect two 3.16 MOhm resistors to the V-pin for the required UV/OV threshold
103	BROWN-IN ACTUAL			52.8 - 80.7	V	Actual AC RMS brown-in range
104	BROWN-OUT ACTUAL			40.0 - 68.5	V	Actual AC RMS brown-out range
106	**LINE OVERVOLTAGE**					
107	OV_TARGET			424.2	V	AC RMS line voltage at which overvoltage will trigger. For High Line desings, brown-in threshold might need to be lowered to get the required overvoltage
	RV_BIAS_ENABLED	AUTO		YES		Resistor between BPP and V pins to increase Line OV threshold without increasing Line UV
	RV_BIAS			357	kΩ	Biasing resistor between BPP and V pins of the device
	OVERVOLTAGE_LINE		Warning	425 - 495	V	The device voltage stress will be 810V when overvoltage is trigerred. It is recommended to keep the stress below 810V
109	**BIAS DIODE**					
110	VBIAS			12.0	V	Rectified bias voltage
111	VF_BIAS			0.70	V	Bias winding diode forward drop

112	VREVERSE_BIASDIODE			126.69	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
113	CBIAS			22	uF	Bias winding rectification capacitor
114	CBPP			4.70	uF	BPP pin capacitor
118	**SECONDARY COMPONENTS**					
119	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
120	RFB_LOWER			11.80	kΩ	Lower feedback resistor
121	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
132	**MULTIPLE OUTPUT PARAMETERS**					
133	OUTPUT 1					
134	VOUT1			12.00	V	Output 1 voltage
135	IOUT1			5.00	A	Output 1 current
136	POUT1			60.00	W	Output 1 power
137	IRMS_SECONDARY1			7.215	A	Root mean squared value of the secondary current for output 1
138	CM_SECONDARY1			1443	Cmils	Bare conductor effective area in circular mils for output 1
139	NSECONDARY1			5		Number of turns for output 1
140	VREVERSE_RECTIFIER1			107.58	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
141	SRFET1	AUTO		AON7254		Secondary rectifier (Logic MOSFET) for output 1
142	VF_SRFET1			0.330	V	SRFET on-time drain voltage for output 1
143	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
144	RDSON_SRFET1			66.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1

9 Performance Data

All the performance data has been taken from the board unless otherwise specifically mentioned.

9.1 Full-Load Efficiency vs. Line

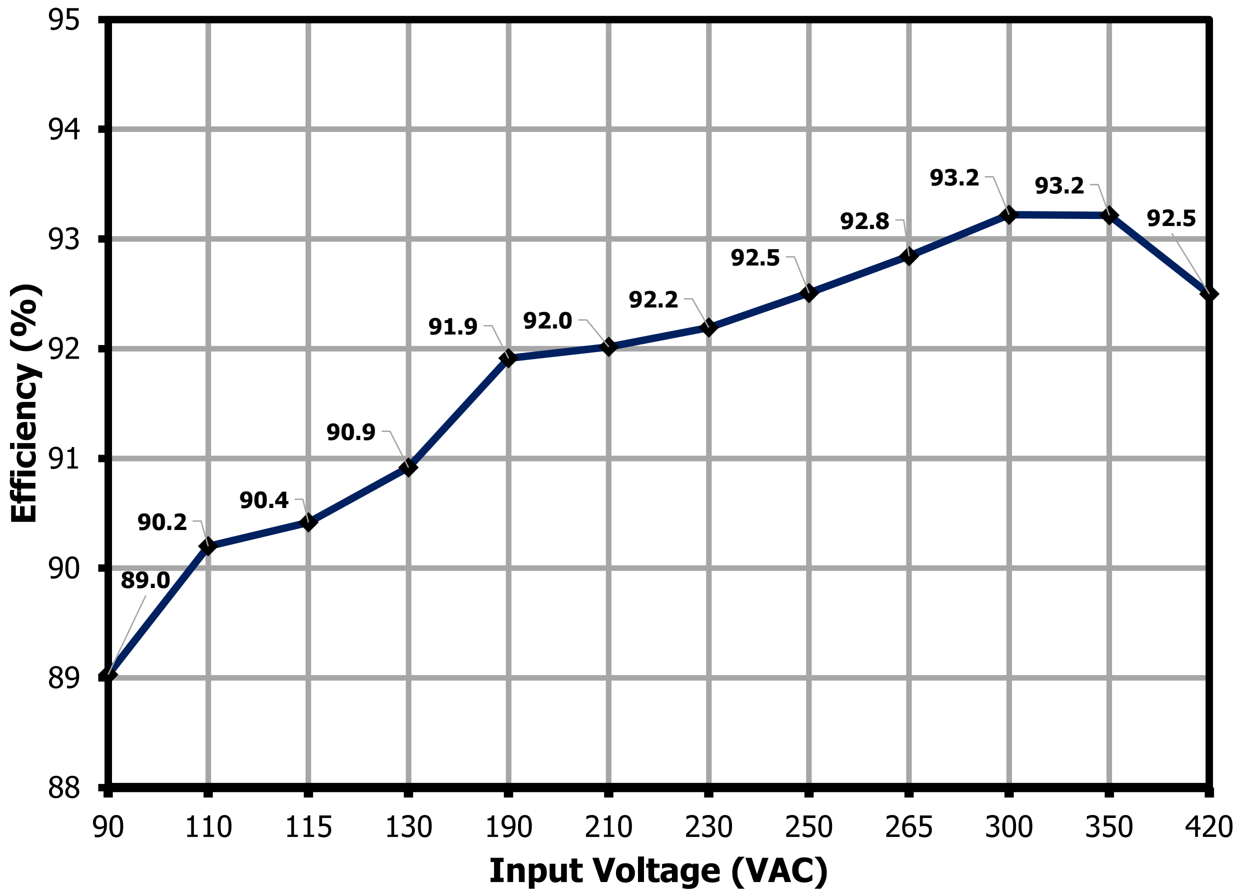


Figure 8 – Full-Load Efficiency vs. Line, Room Ambient.

9.2 Efficiency vs. Load

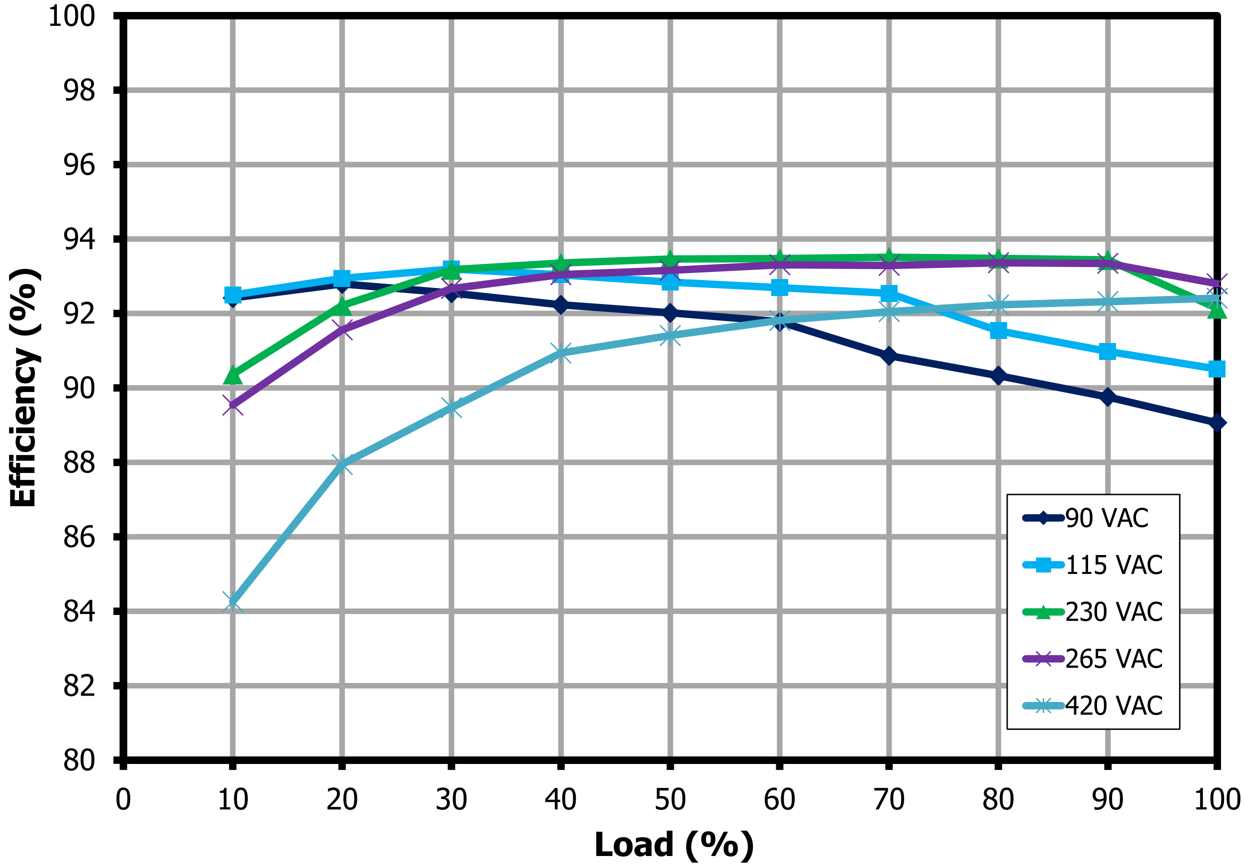


Figure 9 – Efficiency vs. Load, Room Ambient.

9.3 Average Efficiency

	Test	Average	Average	10% Load
Output Voltage (V)	**Power [W]**	**DOE6 Limit (%)**	**CoC v5 Tier 2 (%)**	**CoC v5 Tier 2 (%)**
12	60	88.00	89.00	79.00

9.3.1 Average and 10% Efficiency at 90 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	67.21	59.84	89.03	91.03
75	49.83	45.10	90.50	
50	32.67	30.04	91.95	
25	16.36	15.16	92.62	
10	6.54	6.04	92.26	

9.3.2 Average and 10% Efficiency at 115 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	66.30	59.97	90.45	92.13
75	49.09	45.17	92.01	
50	32.45	30.12	92.83	
25	16.26	15.15	93.21	
10	6.54	6.05	92.52	

9.3.3 Average and 10% Efficiency at 230 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	65.38	60.22	92.11	92.82
75	48.50	45.32	93.45	
50	32.39	30.25	93.40	
25	16.45	15.19	92.33	
10	6.69	6.04	90.25	

9.3.4 Average and 10% Efficiency at 265 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	64.94	60.23	92.75	92.78
75	48.51	45.27	93.31	
50	32.46	30.25	93.19	
25	16.53	15.19	91.88	
10	6.77	6.05	89.45	

9.3.5 Average and 10% Efficiency at 420 VAC Input

% Load	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	65.07	60.12	92.39	91.17
75	49.33	45.42	92.07	
50	33.11	30.27	91.42	
25	17.10	15.18	88.78	
10	7.19	6.06	84.31	

9.4 No-Load Input Power

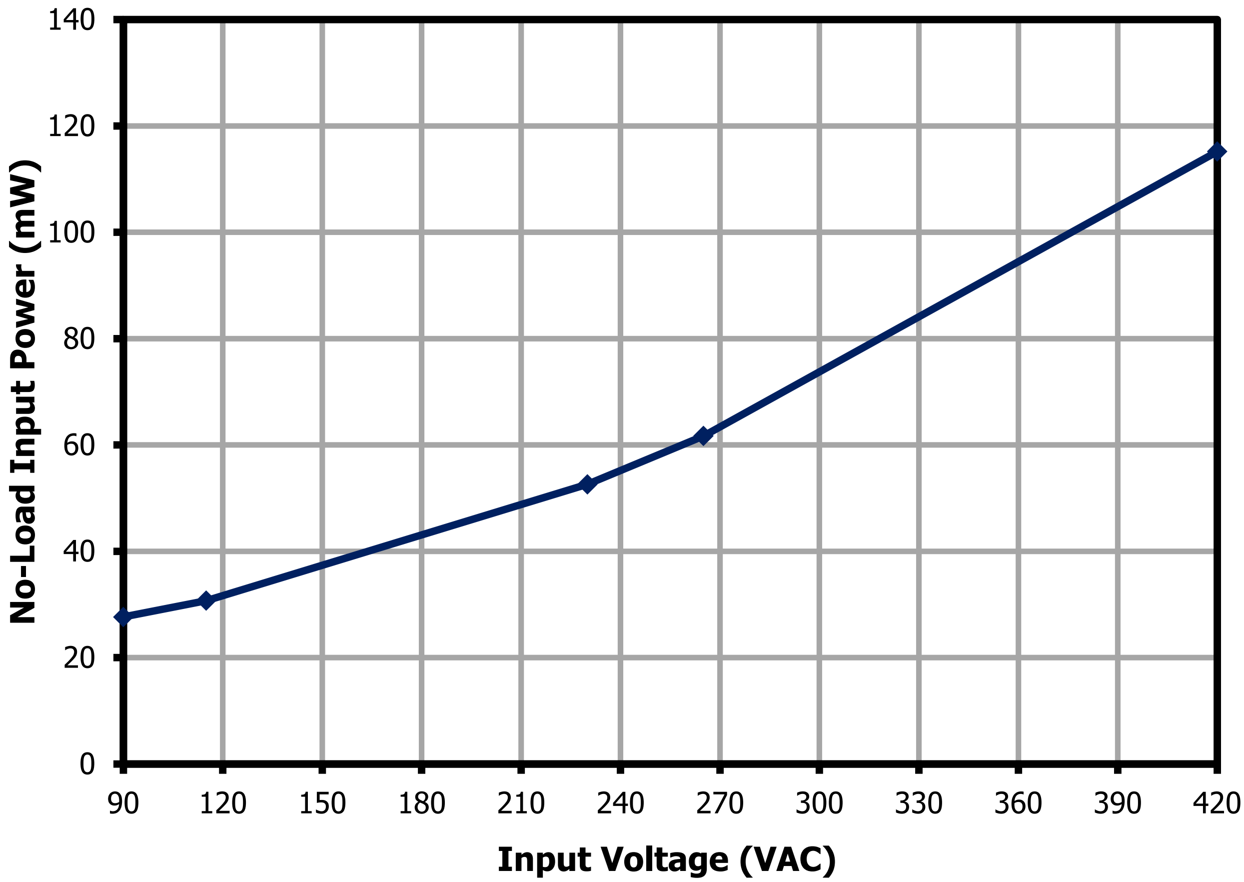


Figure 10 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

9.5 Full-Load Line Regulation

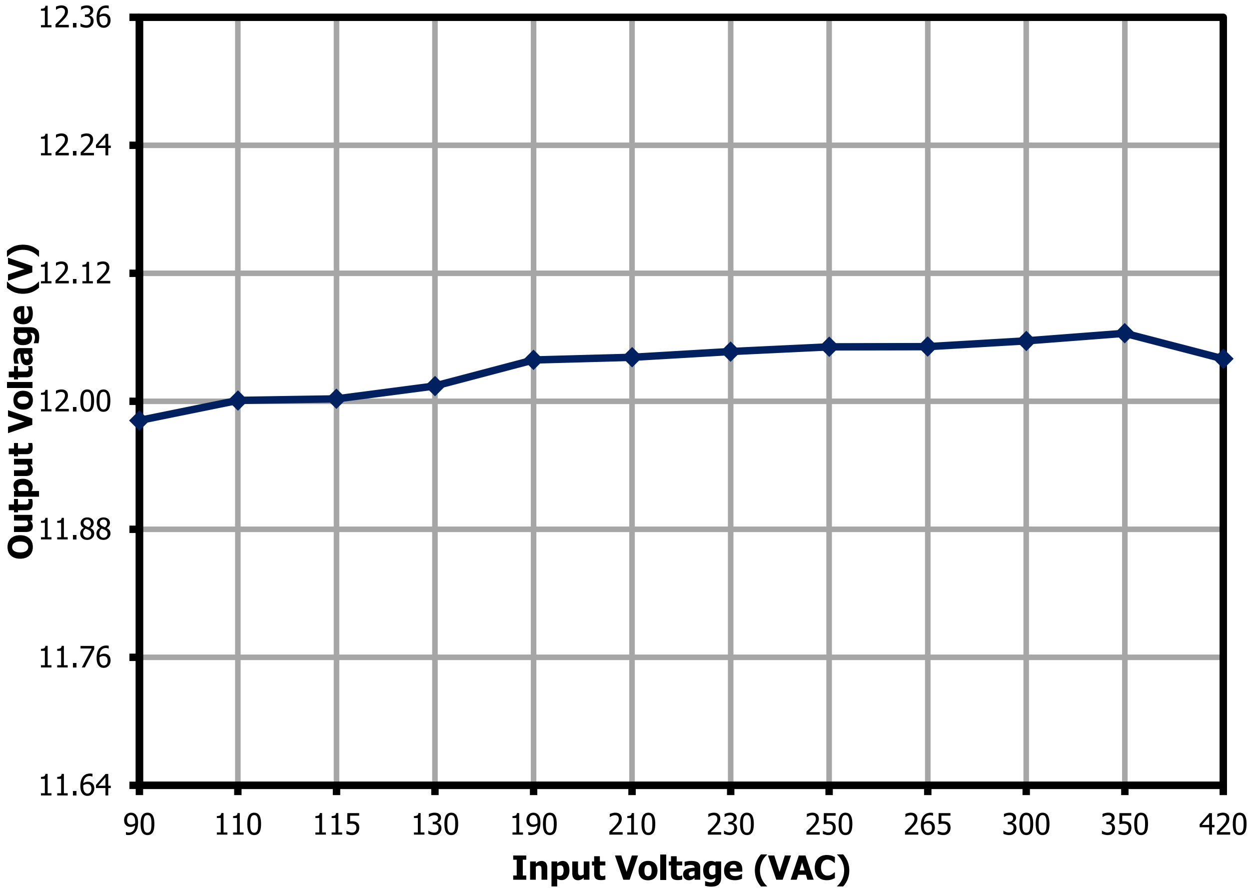


Figure 11 – Full-Load Line Regulation.

9.6 Load Regulation

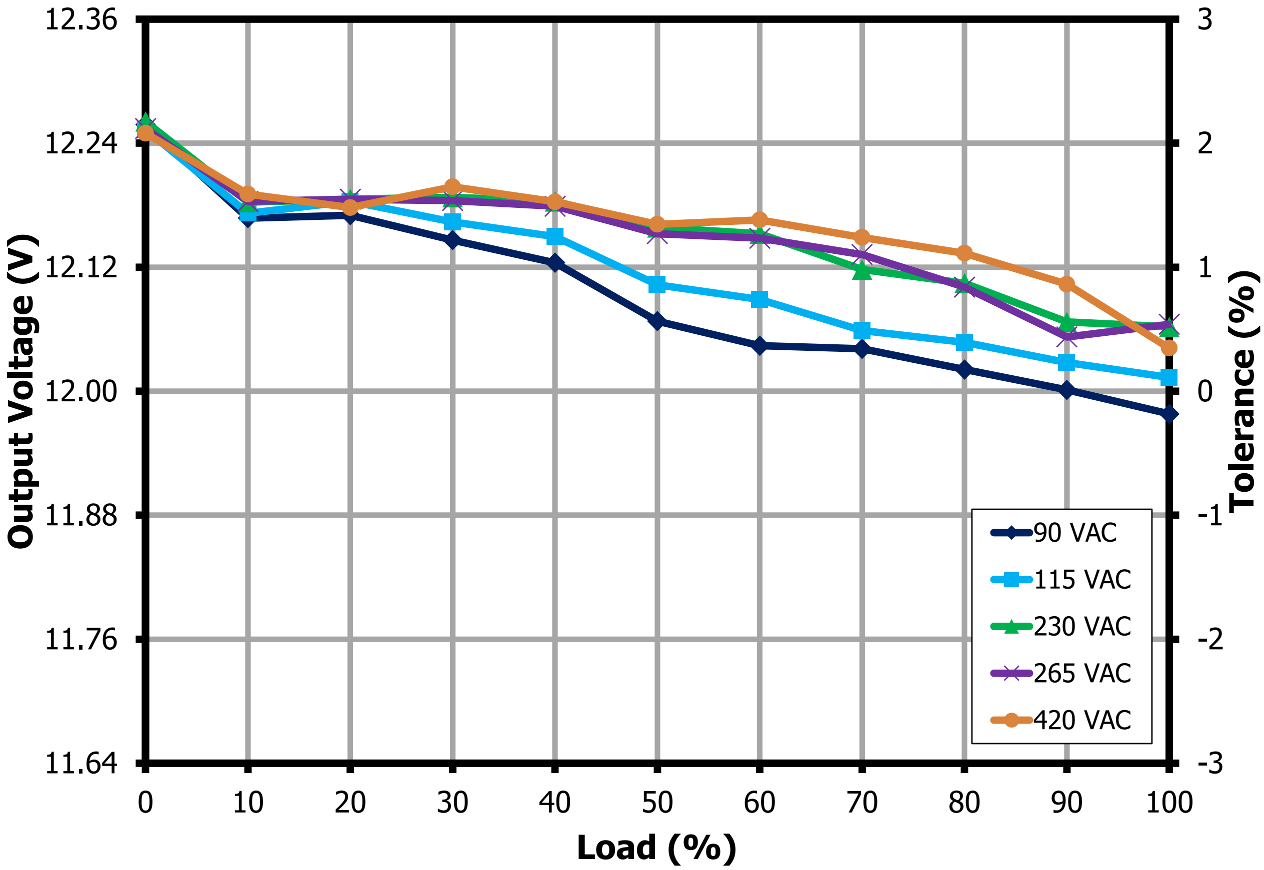


Figure 12 – Load Regulation.

9.7 Standby Output Power

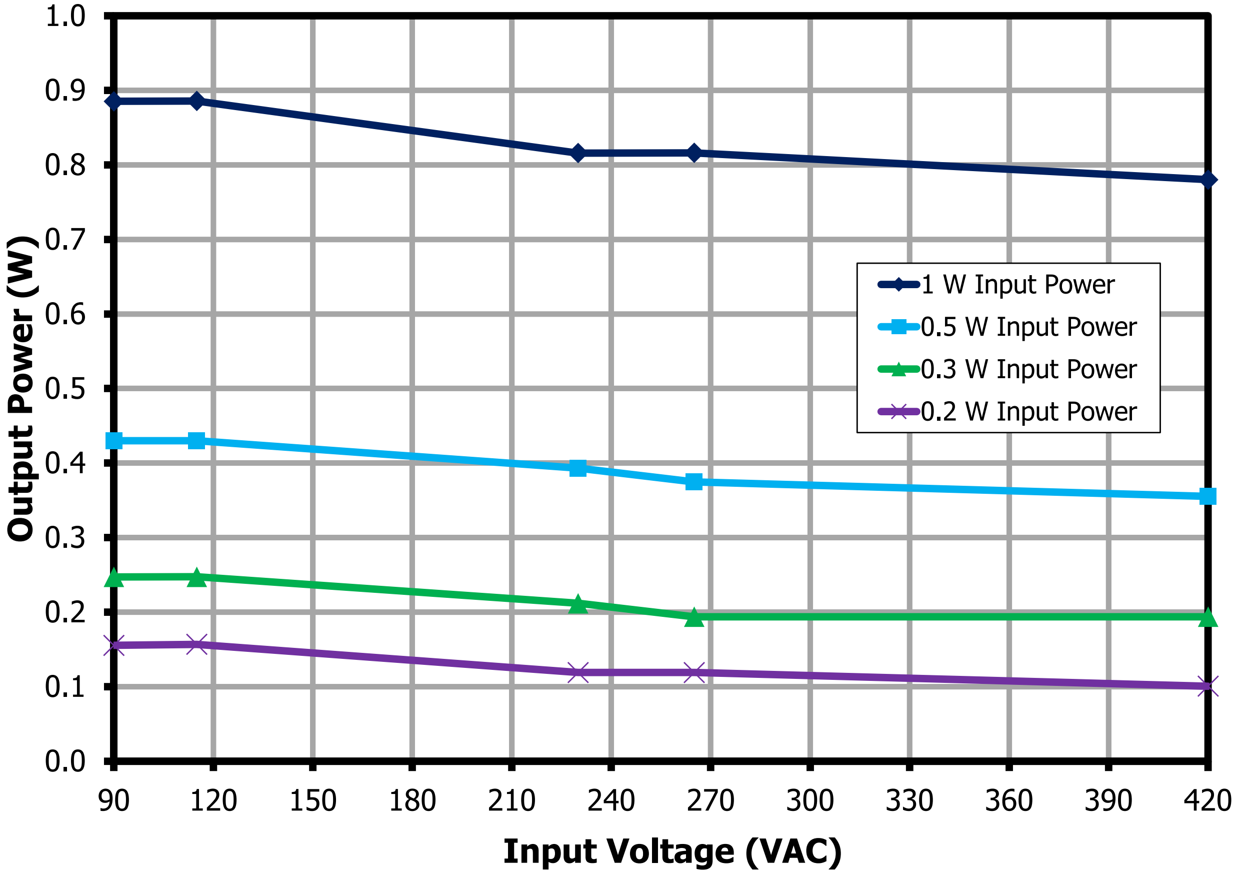


Figure 13 – Standby Output Power.

10 Thermal Performance

Thermal performance is measured inside a thermal chamber at ambient temp of 0 ºC, 25 ºC and 40 ºC using a data logger.

10.1 90 VAC, 60 W at 0 ºC Ambient

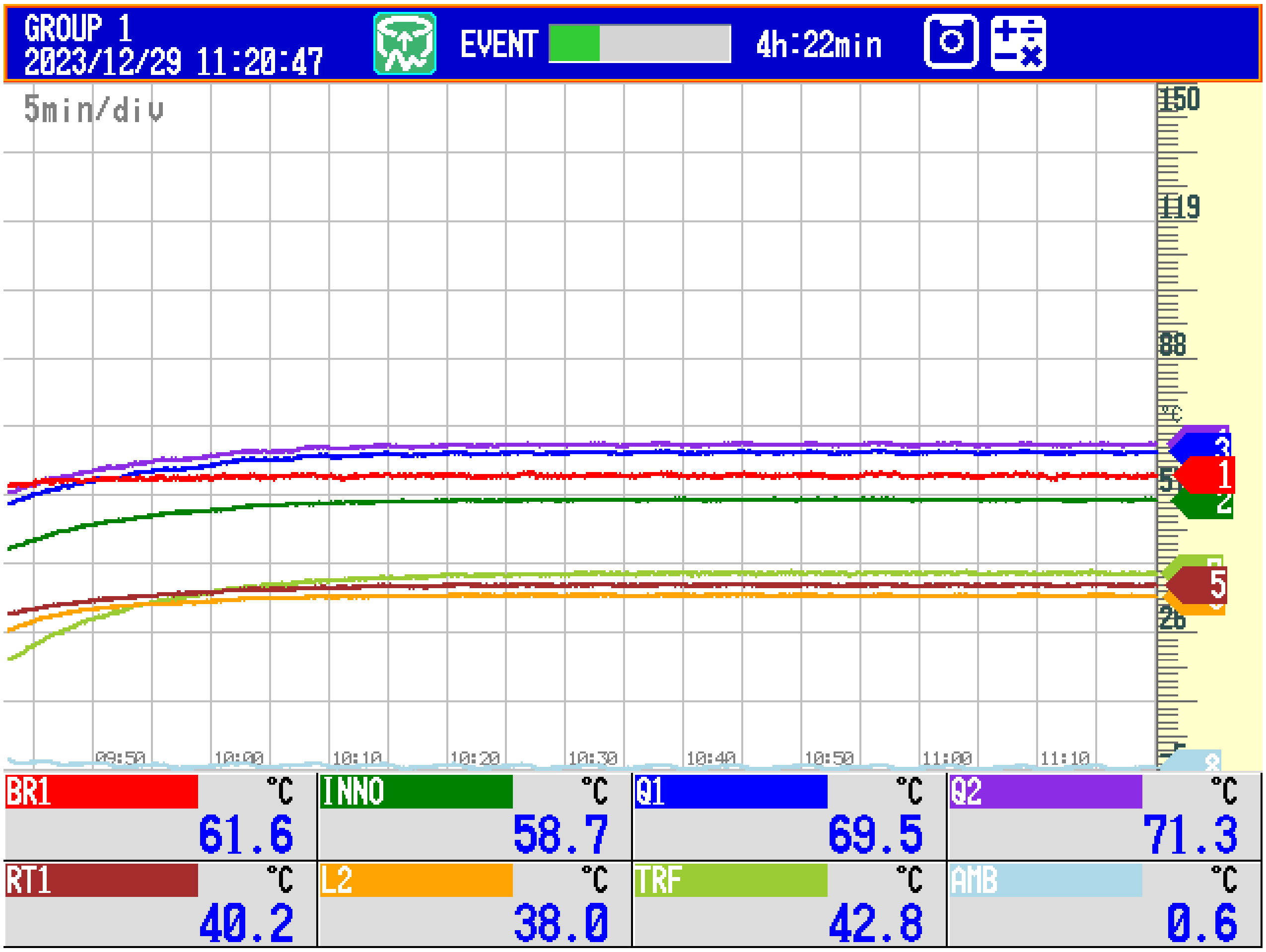


Figure 14 – Thermal Performance at 90 VAC Input.

Component	Temperature (ºC)
Bridge Diode (BR1)	61.6
InnoSwitch (U1)	58.7
SRFET (Q1)	69.5
SRFET (Q2)	71.3
Thermistor (RT1)	40.2
CMC (L2)	38.0
Transformer Core (T1)	42.8
Ambient	0.6

10.2 420 VAC, 60 W at 0 ºC Ambient

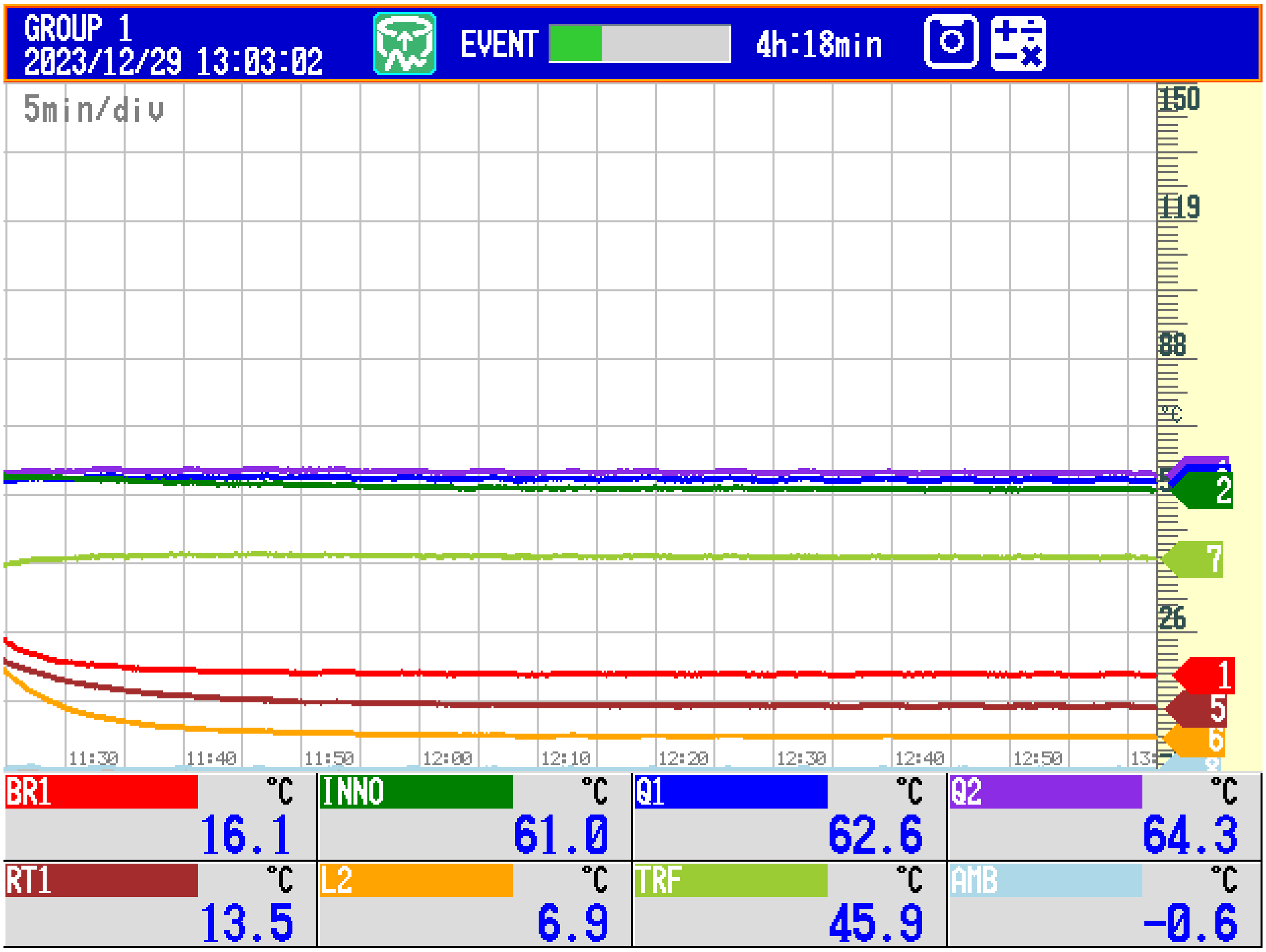


Figure 15 – Thermal Performance at 420 VAC Input.

Component	Max Temperature (ºC)
Bridge Diode (BR1)	16.1
InnoSwitch (U1)	61.0
SRFET (Q1)	62.6
SRFET (Q2)	64.3
Thermistor (RT1)	13.5
CMC (L2)	6.9
Transformer Core (T1)	45.9
Ambient	-0.6

10.3 90 VAC, 60 W at 25 ºC Ambient

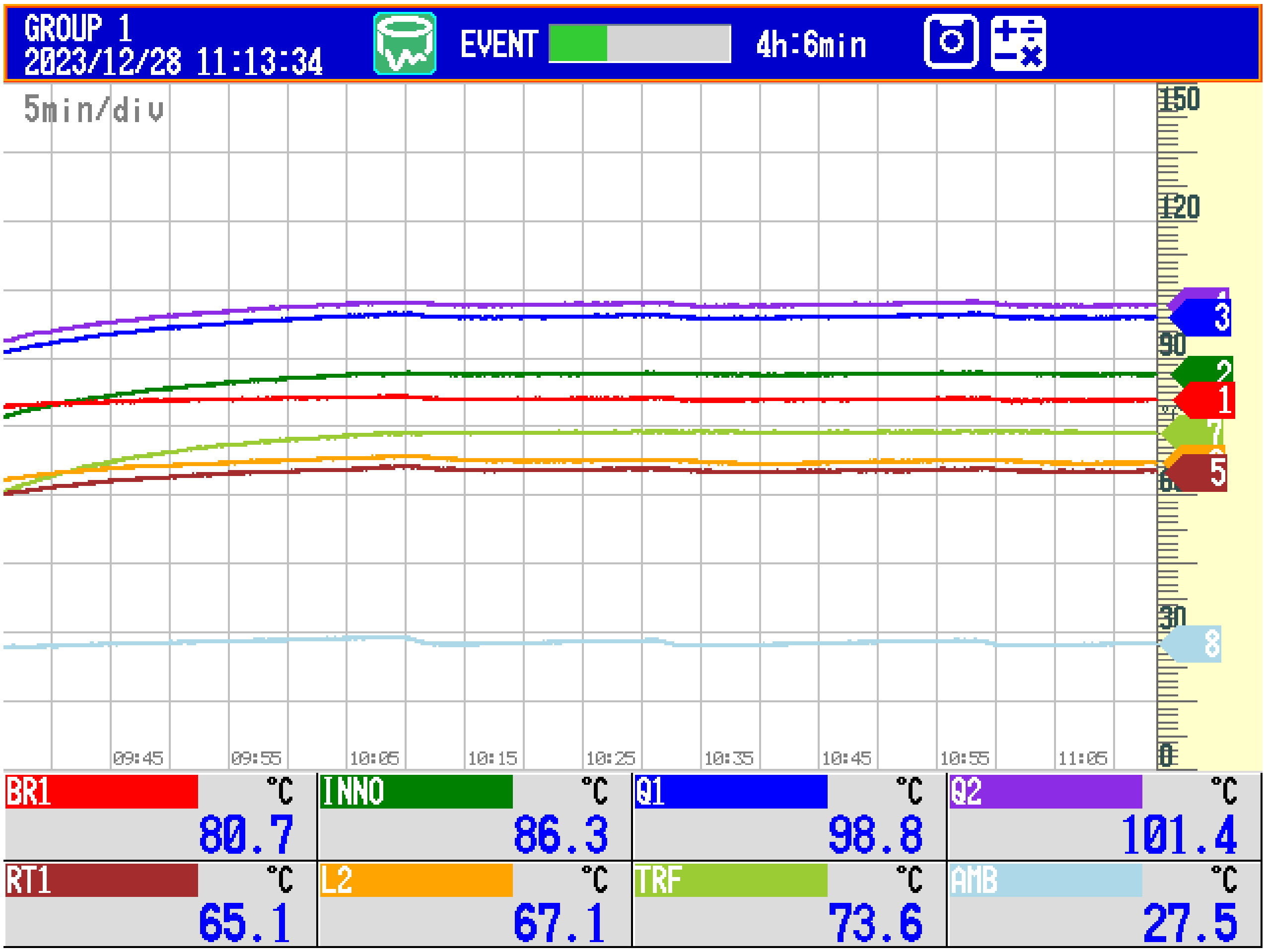


Figure 16 – Thermal Performance at 90 VAC Input.

Component	Max Temperature (ºC)
Bridge Diode (BR1)	80.7
InnoSwitch (U1)	86.3
SRFET (Q1)	98.8
SRFET (Q2)	101.4
Thermistor (RT1)	65.1
CMC (L2)	67.1
Transformer Core (T1)	73.6
Ambient	27.5

10.4 420 VAC Input, 60 W at 25 ºC Ambient

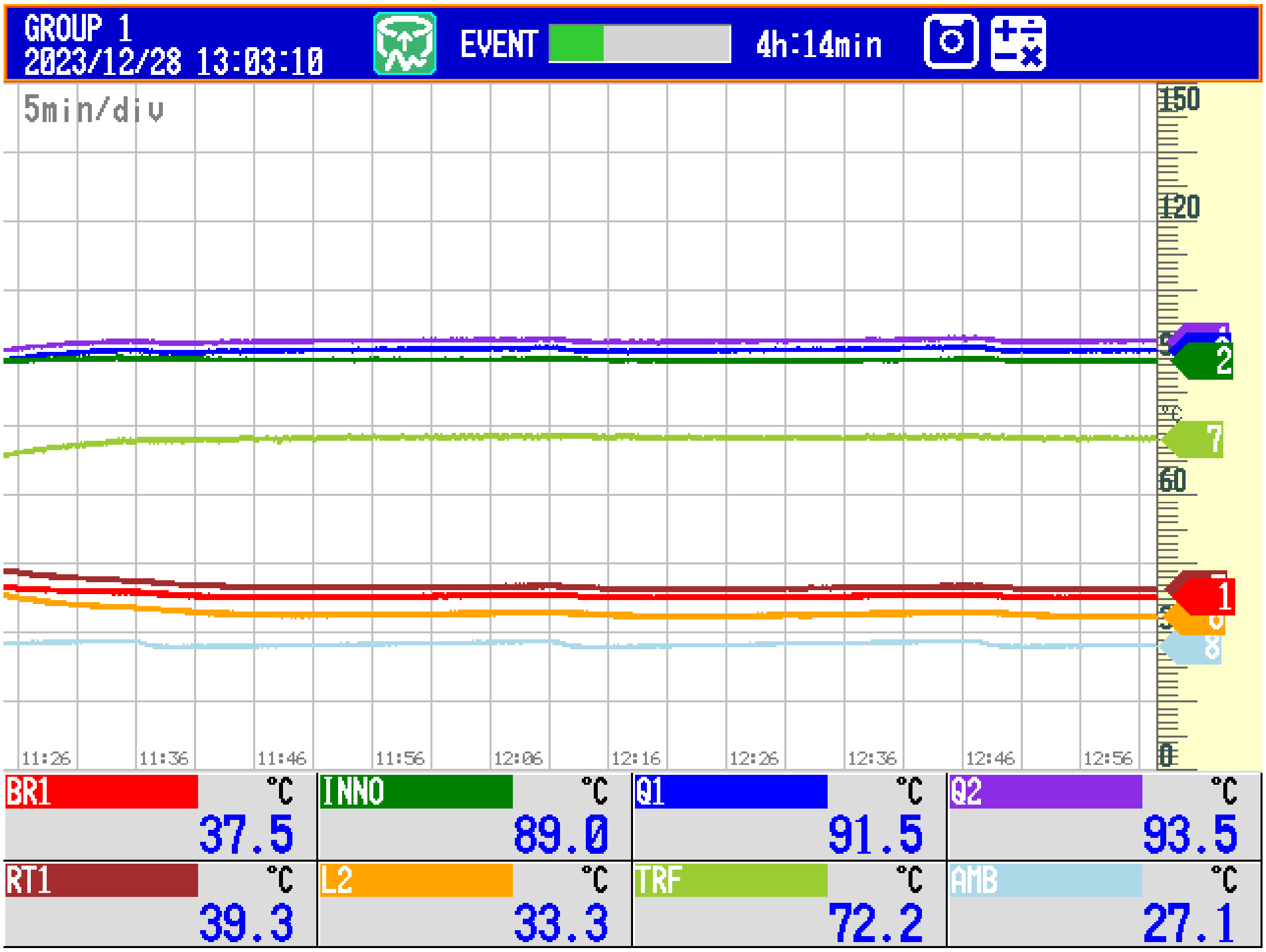


Figure 17 – Thermal Performance at 420 VAC Input.

Component	Max Temperature (ºC)
Bridge Diode (BR1)	37.5
InnoSwitch (U1)	89.0
SRFET (Q1)	91.5
SRFET (Q2)	93.5
Thermistor (RT1)	39.3
CMC (L2)	33.3
Transformer Core (T1)	72.2
Ambient	27.1

10.5 90 VAC Input, 60 W at 40 ºC Ambient

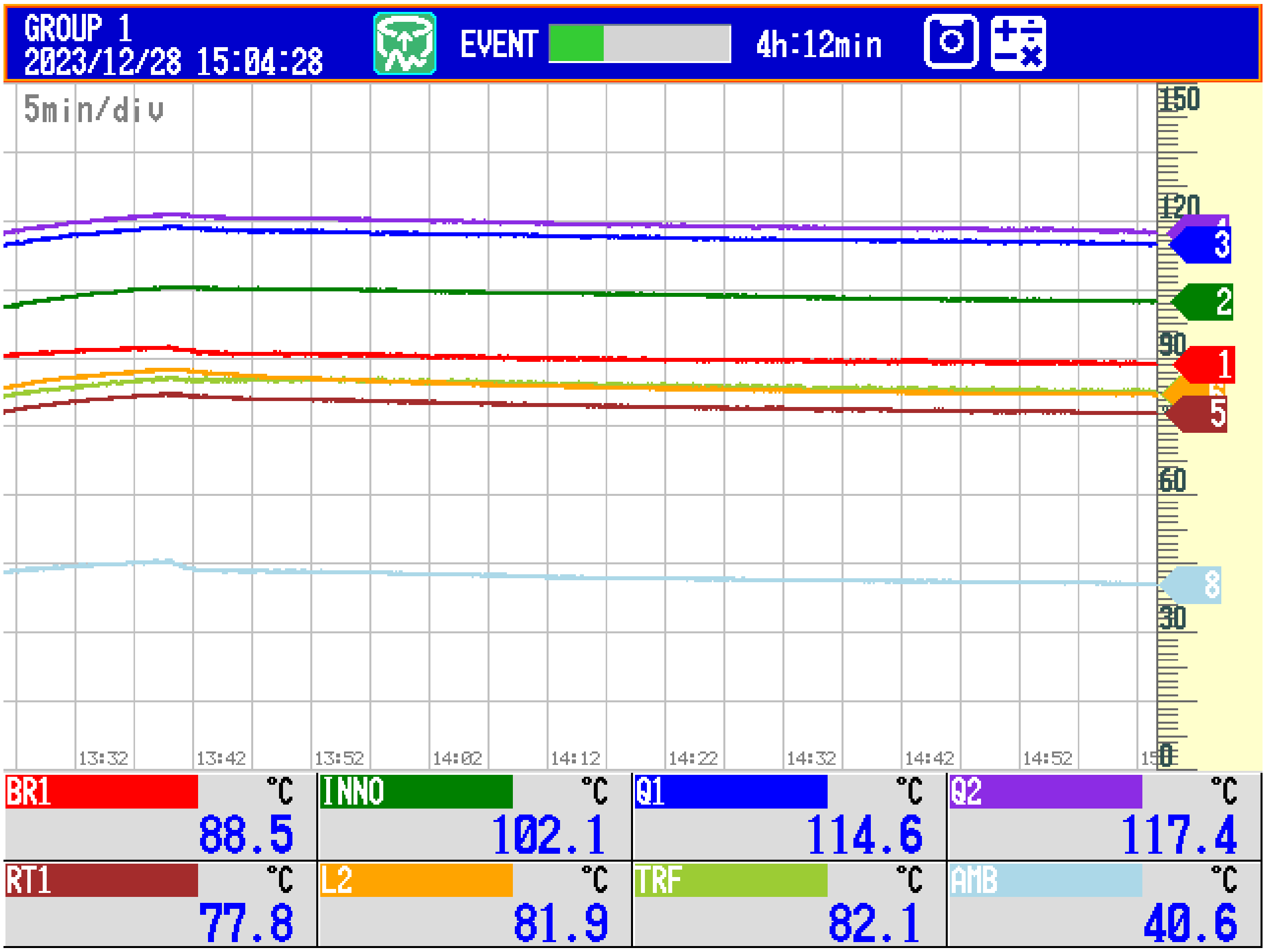


Figure 18 – Thermal Performance at 90 VAC Input.

Component	Max Temperature (ºC)
Bridge Diode (BR1)	88.5
InnoSwitch (U1)	102.1
SRFET (Q1)	114.6
SRFET (Q2)	117.4
Thermistor (RT1)	77.8
CMC (L2)	81.9
Transformer Core (T1)	82.1
Ambient	40.6

10.6 420 VAC Input, 60 W at 40 ºC Ambient

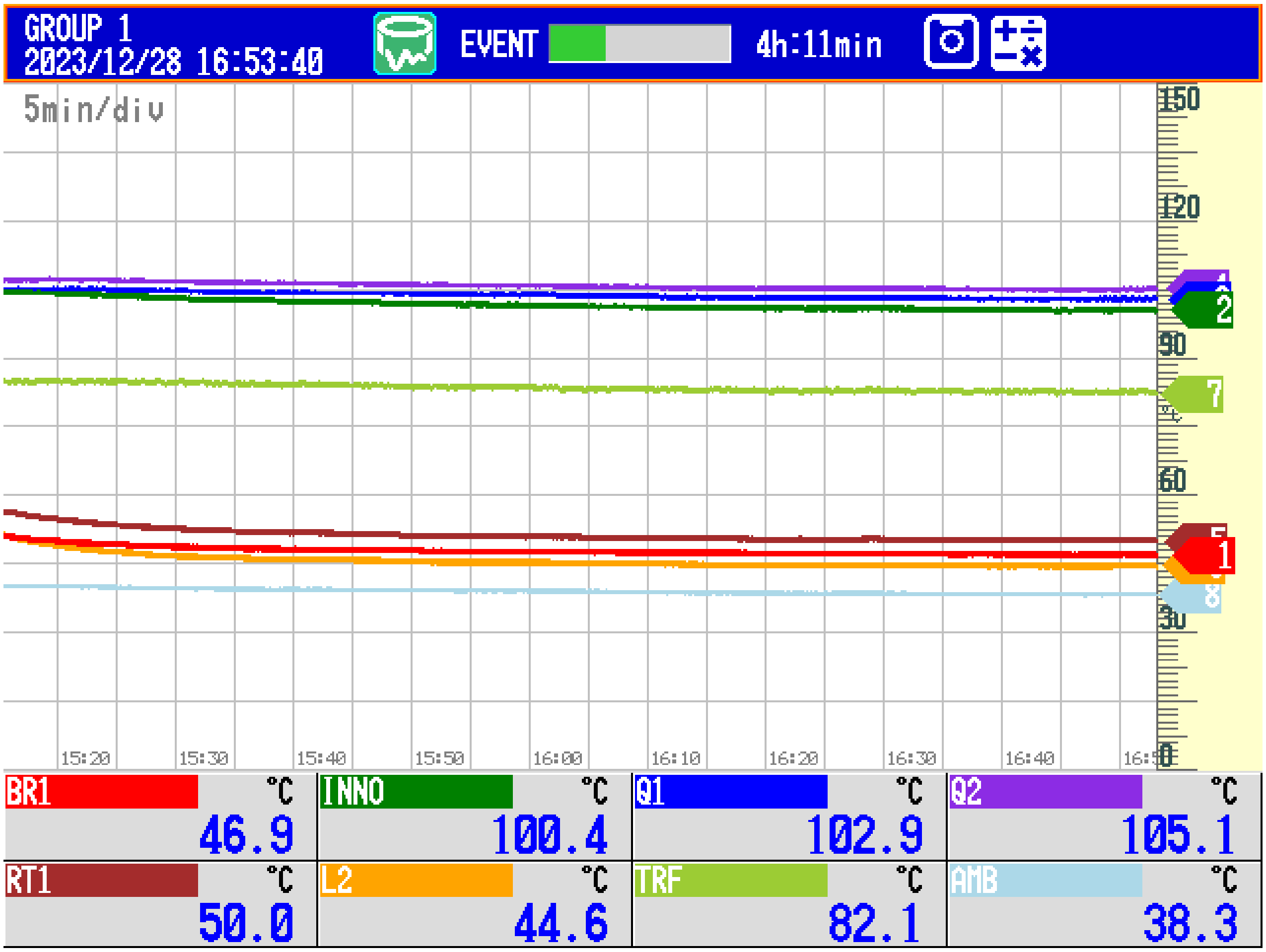


Figure 19 – Thermal Performance at 420 VAC Input.

Component	Max Temperature (ºC)
Bridge Diode (BR1)	46.9
InnoSwitch (U1)	100.4
SRFET (Q1)	102.9
SRFET (Q2)	105.1
Thermistor (RT1)	50.0
CMC (L2)	44.6
Transformer Core (T1)	82.1
Ambient	38.3

11 Waveforms

11.1 Output Voltage Start-up Waveforms at Room Temperature

11.1.1 CC Load

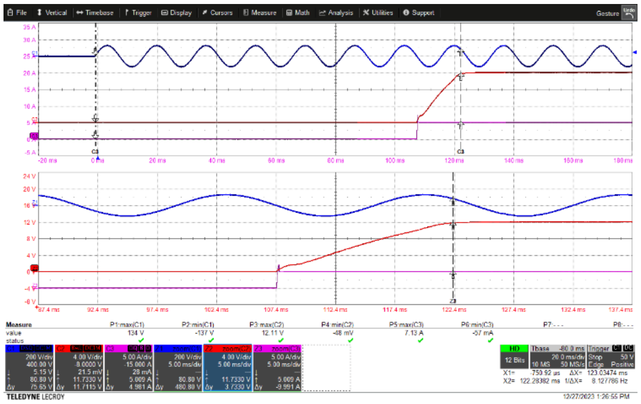


Figure 20 – 90 VAC 60 Hz, I_{OUT} = 5 A.
CH1: Input Voltage: 200 V / div., 20 ms / div.
CH2: Output Voltage: 4 V / div., 20 ms / div.
CH3: Output Current: 5 A / div., 20 ms / div.
Zoom: 5 ms / div.
Output Voltage, Max = 12.11 V.
Output Voltage, Rise Time = 14.89 ms.
Start-up Time = 123.0 ms.

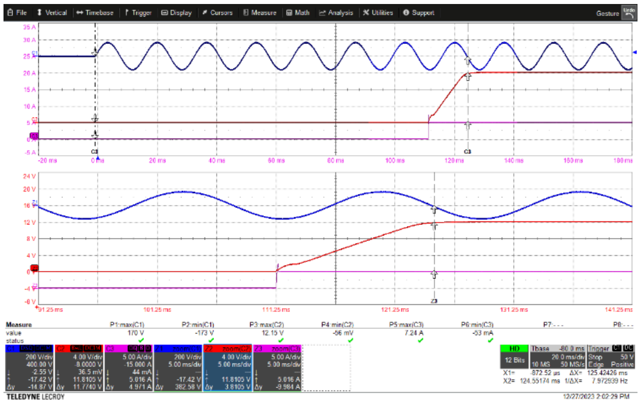


Figure 21 – 115 VAC 60 Hz, I_{OUT} = 5 A.
CH1: Input Voltage: 200 V / div., 20 ms / div.
CH2: Output Voltage: 4 V / div., 20 ms / div.
CH3: Output Current: 5 A / div., 20 ms / div.
Zoom: 5 ms / div.
Output Voltage, Max = 12.15 V.
Output Voltage, Rise Time = 13.35 ms.
Start-up Time = 125.42 ms.

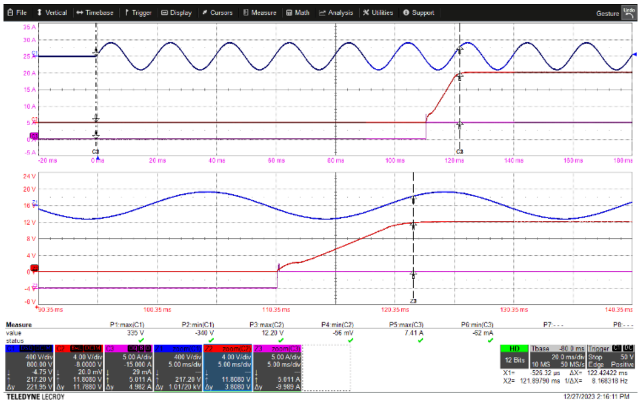


Figure 22 – 230 VAC 60 Hz, I_{OUT} = 5 A.
CH1: Input Voltage: 400 V / div., 20 ms / div.
CH2: Output Voltage: 4 V / div., 20 ms / div.
CH3: Output Current: 5 A / div., 20 ms / div.
Zoom: 5 ms / div.
Output Voltage, Max = 12.20 V.
Output Voltage, Rise Time = 11.53 ms.
Start-up Time = 122.42 ms.

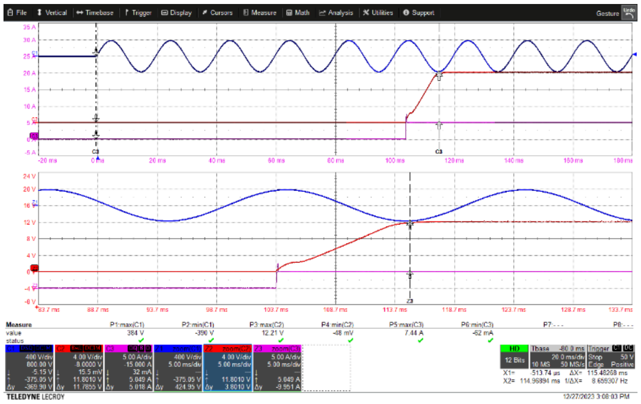


Figure 23 – 265 VAC 60 Hz, I_{OUT} = 5 A.
CH1: Input Voltage: 400 V / div., 20 ms / div.
CH2: Output Voltage: 4 V / div., 20 ms / div.
CH3: Output Current: 5 A / div., 20 ms / div.
Zoom: 5 ms / div.
Output Voltage, Max = 12.21 V.
Output Voltage, Rise Time = 11.29 ms.
Start-up Time = 115.48 ms.

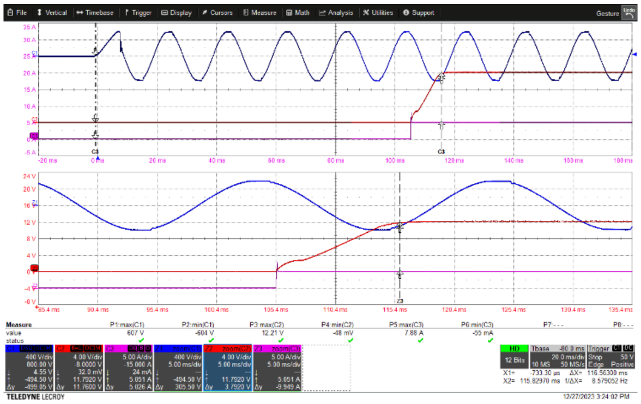


Figure 24 – 420 VAC 60 Hz, I_{OUT} = 5 A.
CH1: Input Voltage: 400 V / div., 20 ms / div.
CH2: Output Voltage: 4 V / div., 20 ms / div.
CH3: Output Current: 5 A / div., 20 ms / div.
Zoom: 5 ms / div.
Output Voltage, Max = 12.21 V.
Output Voltage, Rise Time = 10.45 ms.
Start-up Time = 116.56 ms.

11.1.2 CR Load

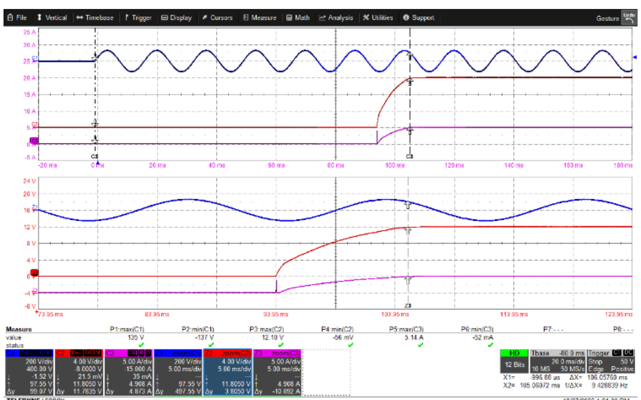


Figure 25 – 90 VAC 60 Hz, Ro = 2.4 Ω (Full-Load, CR).
CH1: Input Voltage: 200 V / div., 20 ms / div.
CH2: Output Voltage: 4 V / div., 20 ms / div.
CH3: Output Current: 5 A / div., 20 ms / div.
Zoom: 5 ms / div.
Output Voltage, Max = 12.10 V.
Output Voltage, Rise Time = 11.12 ms.
Start-up Time = 106.06 ms.

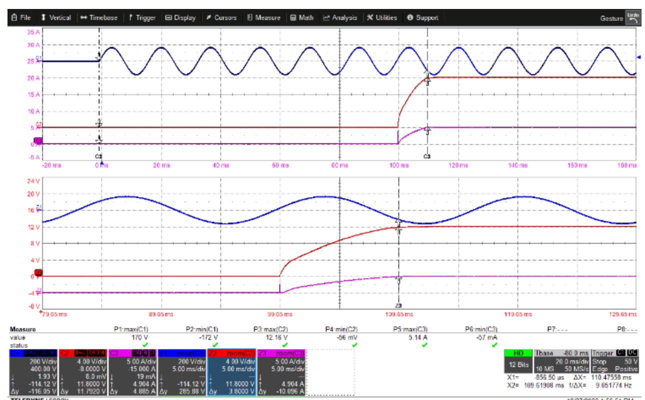


Figure 26 – 115 VAC 60 Hz, Ro = 2.4 Ω (Full-Load, CR).
CH1: Input Voltage: 200 V / div., 20 ms / div.
CH2: Output Voltage: 4 V / div., 20 ms / div.
CH3: Output Current: 5 A / div., 20 ms / div.
Zoom: 5 ms / div.
Output Voltage, Max = 12.16 V.
Output Voltage, Rise Time = 10.03 ms.
Start-up Time = 110.48 ms.

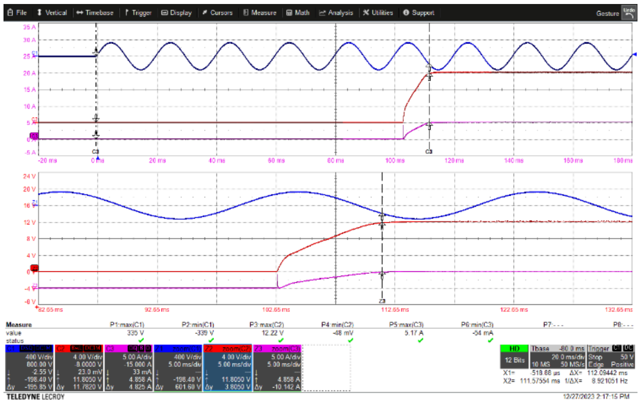


Figure 27 – 230 VAC 60 Hz, Ro = 2.4 Ω (Full-Load, CR).
CH1: Input Voltage: 400 V / div., 20 ms / div.
CH2: Output Voltage: 4 V / div., 20 ms / div.
CH3: Output Current: 5 A / div., 20 ms / div.
Zoom: 5 ms / div.
Output Voltage, Max = 12.22 V.
Output Voltage, Rise Time = 8.85 ms.
Start-up Time = 112.09 ms.

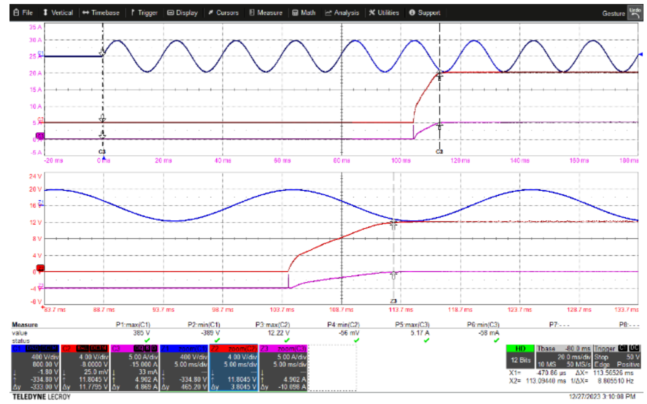


Figure 28 – 265 VAC 60 Hz, Ro = 2.4 Ω (Full-Load, CR).
CH1: Input Voltage: 400 V / div., 20 ms / div.
CH2: Output Voltage: 4 V / div., 20 ms / div.
CH3: Output Current: 5 A / div., 20 ms / div.
Zoom: 5 ms / div.
Output Voltage, Max = 12.09 V.
Output Voltage, Rise Time = 8.93 ms.
Start-up Time = 113.56 ms.

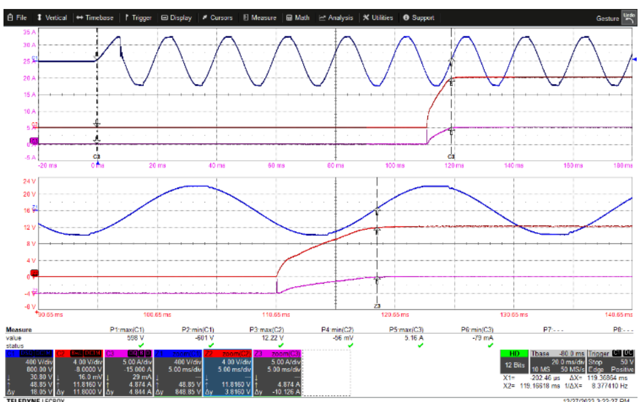


Figure 29 – 420 VAC 60 Hz, Ro = 2.4 Ω (Full-Load, CR).
CH1: Input Voltage: 400 V / div., 20 ms / div.
CH2: Output Voltage: 4 V / div., 20 ms / div.
CH3: Output Current: 5 A / div., 20 ms / div.
Zoom: 5 ms / div.
Output Voltage, Max = 12.22 V.
Output Voltage, Rise Time = 8.51 ms.
Start-up Time = 119.37 ms.

11.2 Load Transient Response (On Board)

11.2.1 0 – 100 % Load Step

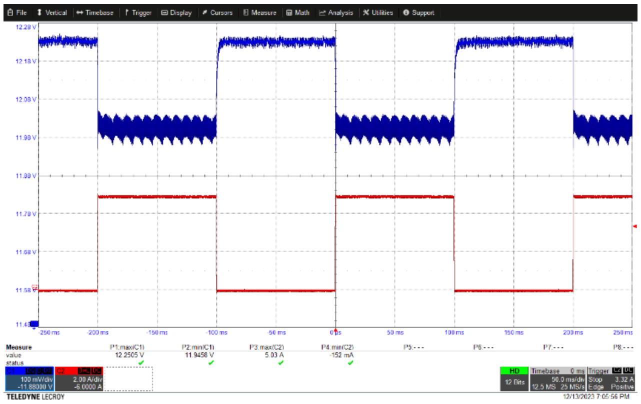


Figure 30 – 90 VAC; I_{OUT} = 0 A – 5 A (0-100%) Load Step.
CH1: Output Voltage: 100 mV / div., 50 ms / div.
CH2: Output Current: 2 A / div., 50 ms / div.
V_{MAX}: 12.25 V.
V_{MIN}: 11.95 V.

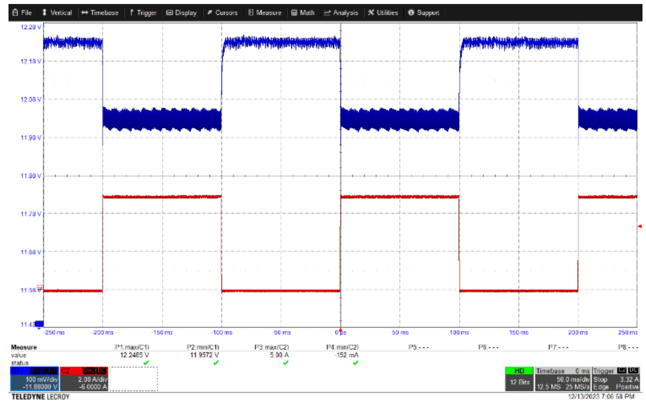


Figure 31 – 115 VAC; I_{OUT} = 0 A – 5 A (0-100%) Load Step.
CH1: Output Voltage: 100 mV / div., 50 ms / div.
CH2: Output Current: 2 A / div., 50 ms / div.
V_{MAX}: 12.25 V.
V_{MIN}: 11.96 V.

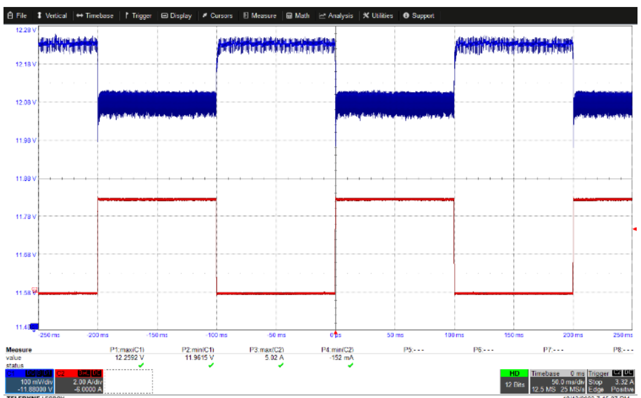


Figure 32 – 230 VAC; I_{OUT} = 0 A – 5 A (0-100%) Load Step.
CH1: Output Voltage: 100 mV / div., 50 ms / div.
CH2: Output Current: 2 A / div., 50 ms / div.
V_{MAX}: 12.26 V.
V_{MIN}: 11.96 V.

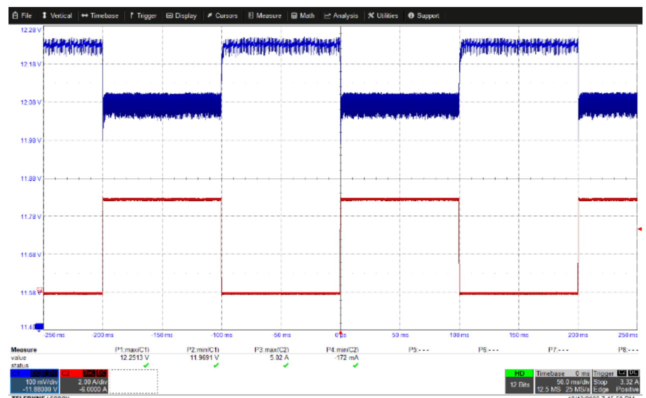


Figure 33 – 265 VAC; I_{OUT} = 0 A – 5 A (0-100%) Load Step.
CH1: Output Voltage: 100 mV / div., 50 ms / div.
CH2: Output Current: 2 A / div., 50 ms / div.
V_{MAX}: 12.25 V.
V_{MIN}: 11.97 V.

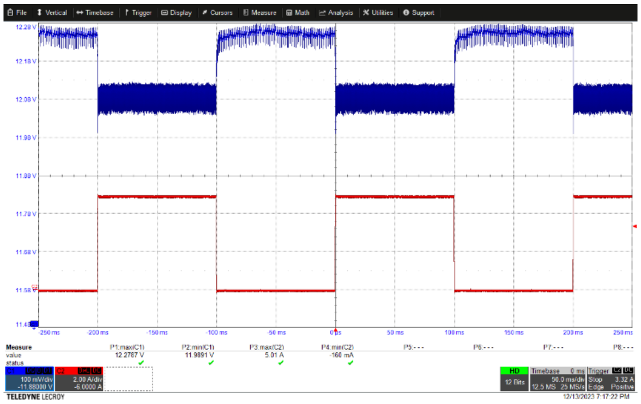


Figure 34 – 420 VAC; I_{OUT} = 0 A – 5 A (0-100%) Load Step.
CH1: Output Voltage: 100 mV / div., 50 ms / div.
CH2: Output Current: 2 A / div., 50 ms / div.
V_{MAX}: 12.28 V.
V_{MIN}: 11.99 V.

11.2.2 50 % – 100 % Load Step

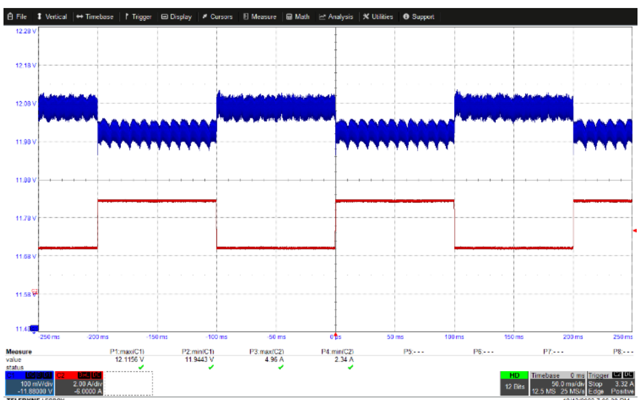


Figure 35 – 90 VAC; I_{OUT} = 2.5 A – 5 A (50-100%) Load Step.
CH1: Output Voltage: 100 mV / div., 50 ms / div.
CH2: Output Current: 2 A / div., 50 ms / div.
V_{MAX}: 12.12 V.
V_{MIN}: 11.94 V.

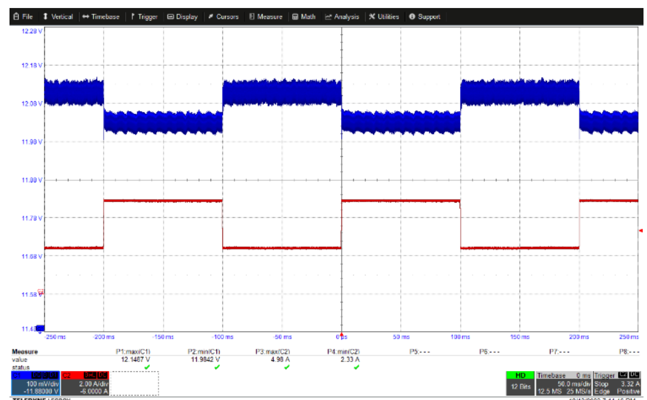


Figure 36 – 115 VAC; I_{OUT} = 2.5 A – 5 A (50-100%) Load Step.
CH1: Output Voltage: 100 mV / div., 50 ms / div.
CH2: Output Current: 2 A / div., 50 ms / div.
V_{MAX}: 12.15 V.
V_{MIN}: 11.98 V.

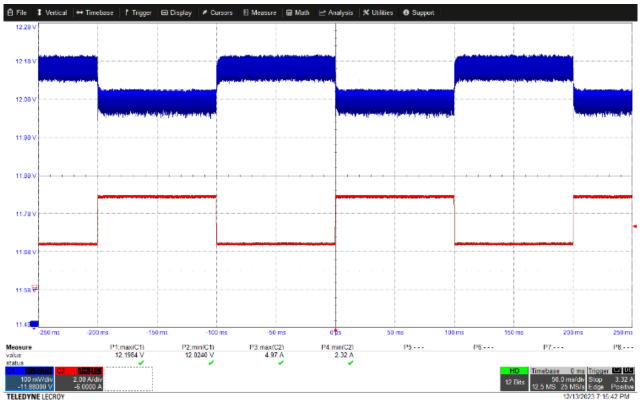


Figure 37 – 230 VAC; I_{OUT} = 2.5 A – 5 A (50-100%) Load Step.
CH1: Output Voltage: 100 mV / div., 50 ms / div.
CH2: Output Current: 2 A / div., 50 ms / div.
V_{MAX}: 12.20 V.
V_{MIN}: 12.02 V.

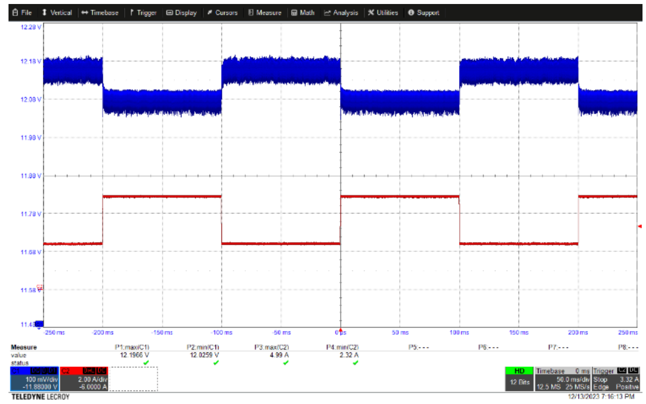


Figure 38 – 265 VAC; I_{OUT} = 2.5 A – 5 A (50-100%) Load Step.
CH1: Output Voltage: 100 mV / div., 50 ms / div.
CH2: Output Current: 2 A / div., 50 ms / div.
V_{MAX}: 12.20 V.
V_{MIN}: 12.03 V.

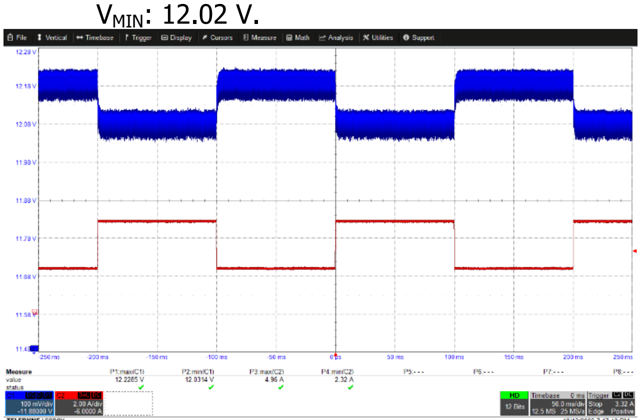


Figure 39 – 420 VAC; I_{OUT} = 2.5 A – 5 A (50-100%) Load Step.
CH1: Output Voltage: 100 mV / div., 50 ms / div.
CH2: Output Current: 2 A / div., 50 ms / div.
V_{MAX}: 12.22 V.
V_{MIN}: 12.03 V.

11.3 Switching Waveforms

11.3.1 Drain Voltage and Current at Start-up Operation

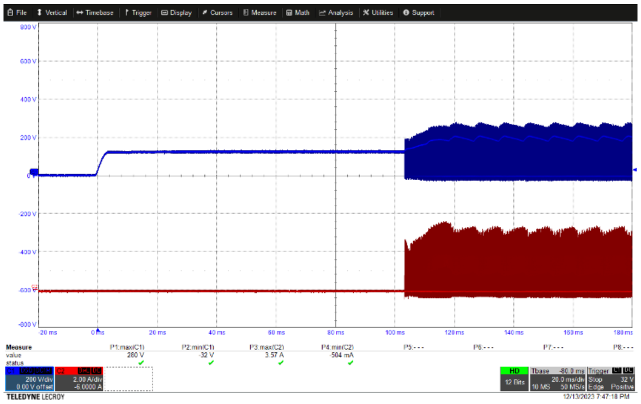


Figure 40 – 90 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 200 V / div., 20 ms / div.
CH 2: Drain Current: 2 A / div., 20 ms / div.
Drain Voltage, Max = 280 V.
Drain Current, Max = 3.57 A.

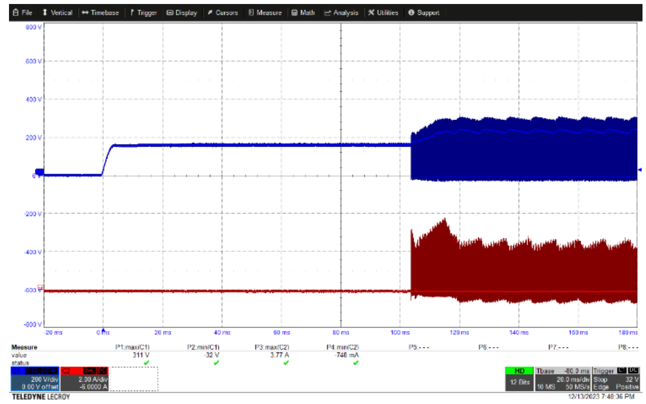


Figure 41 – 115 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 200 V / div., 20 ms / div.
CH 2: Drain Current: 2 A / div., 20 ms / div.
Drain Voltage, Max = 311 V.
Drain Current, Max = 3.77 A.

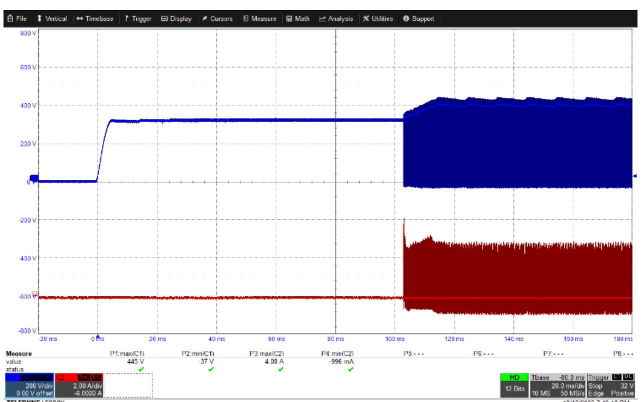


Figure 42 – 230 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 200 V / div., 20 ms / div.
CH 2: Drain Current: 2 A / div., 20 ms / div.
Drain Voltage, Max = 445 V.
Drain Current, Max = 4.08 A.

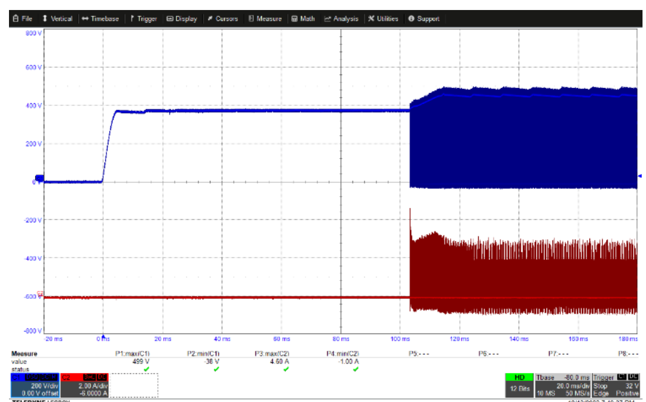


Figure 43 – 265 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 200 V / div., 20 ms / div.
CH 2: Drain Current: 2 A / div., 20 ms / div.
Drain Voltage, Max = 499 V.
Drain Current, Max = 4.60 A.

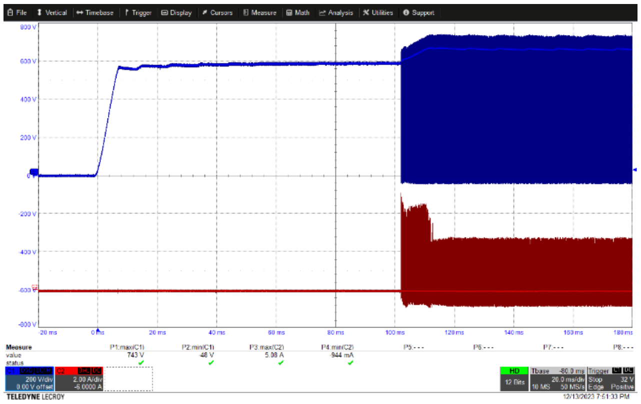


Figure 44 – 420 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 200 V / div., 20 ms / div.
CH 2: Drain Current: 2 A / div., 20 ms / div.
Drain Voltage, Max = 743 V.
Drain Current, Max = 5.08 A.

11.3.2 Drain Voltage and Current at Normal Operation

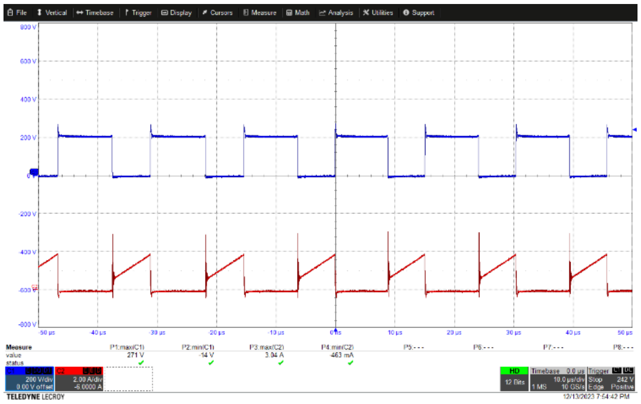


Figure 45 – 90 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 200 V / div., 10 μs / div.
CH 2: Drain Current: 2 A / div., 10 μs / div.
Drain Voltage, Max = 271 V.
Drain Current, Max = 3.04 A.

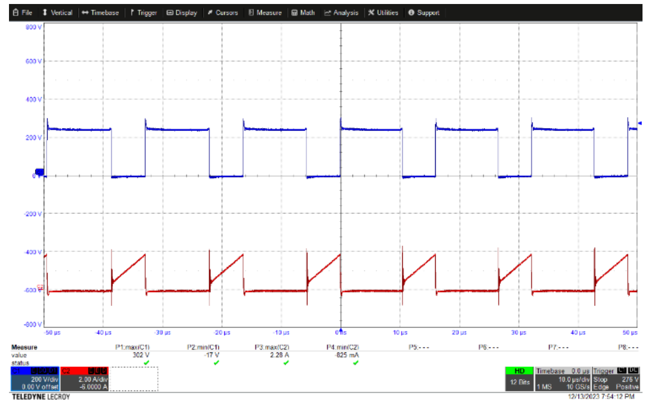


Figure 46 – 115 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 200 V / div., 10 μs / div.
CH 2: Drain Current: 2 A / div., 10 μs / div.
Drain Voltage, Max = 302 V.
Drain Current, Max = 2.28 A.

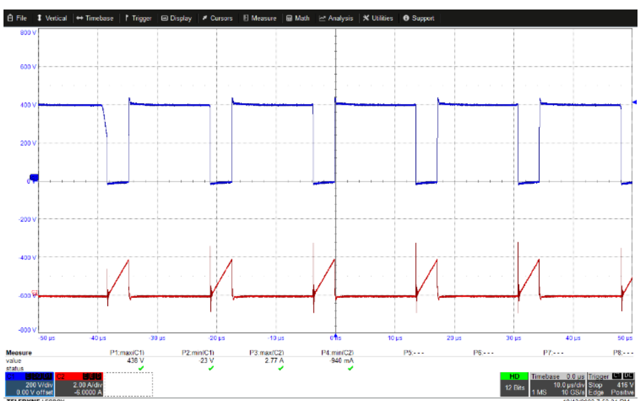


Figure 47 – 230 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 200 V / div., 10 μs / div.
CH 2: Drain Current: 2 A / div., 10 μs / div.
Drain Voltage, Max = 438 V.
Drain Current, Max = 2.77 A.

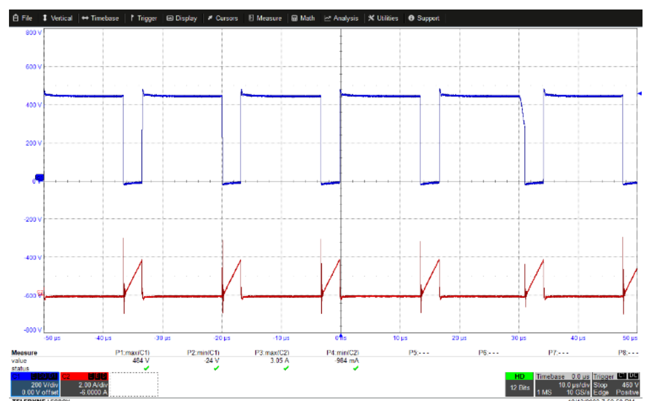


Figure 48 – 265 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 200 V / div., 10 μs / div.
CH 2: Drain Current: 2 A / div., 10 μs / div.
Drain Voltage, Max = 484 V.
Drain Current, Max = 3.05 A.

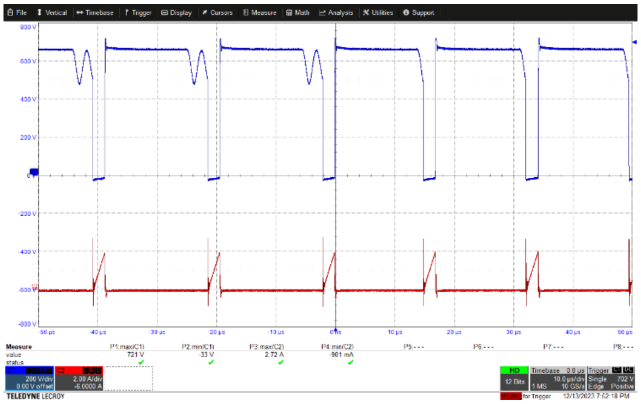


Figure 49 – 420 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 200 V / div., 10 µs / div.
CH 2: Drain Current: 2 A / div., 10 µs / div.
Drain Voltage, Max = 721 V.
Drain Current, Max = 2.72 A.

11.3.3 Drain Voltage and Current with Output Short

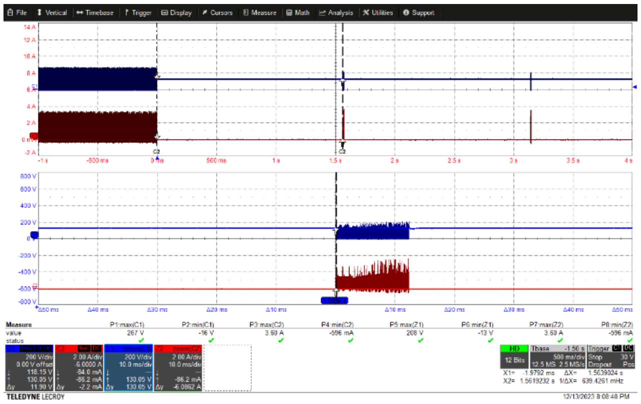


Figure 50 – 90 VAC.
CH1: Drain Voltage: 200 V / div., 500 ms / div.
CH2: Drain Current: 2 A / div., 500 ms / div.
Zoom: 10 ms / div.
Drain Voltage, Max = 267 V.
Drain Current, Max = 3.60 A.

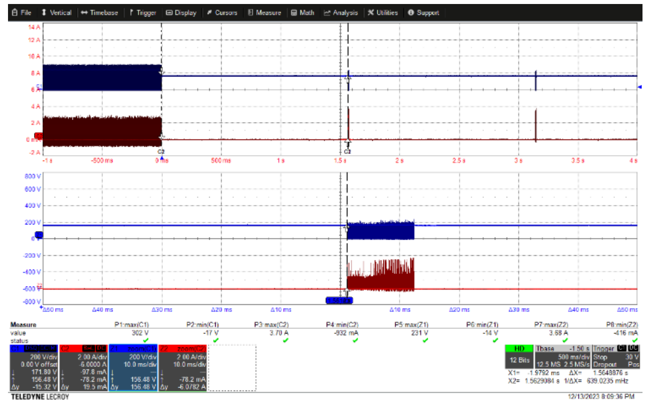


Figure 51 – 115 VAC.
CH1: Drain Voltage: 200 V / div., 500 m s/ div.
CH2: Drain Current: 2 A / div., 500 ms / div.
Zoom: 10 ms / div.
Drain Voltage, Max = 302 V.
Drain Current, Max = 3.70 A.

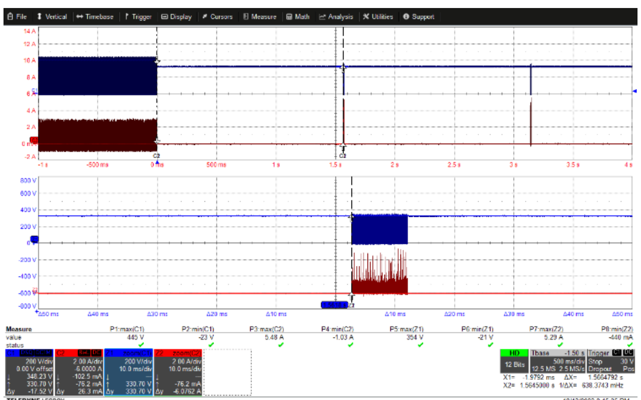


Figure 52 – 230 VAC.
CH1: Drain Voltage: 200 V / div., 500 ms / div.
CH2: Drain Current: 2 A / div., 500 ms / div.
Zoom: 10 ms / div.
Drain Voltage, Max = 445 V.
Drain Current, Max = 5.48 A.

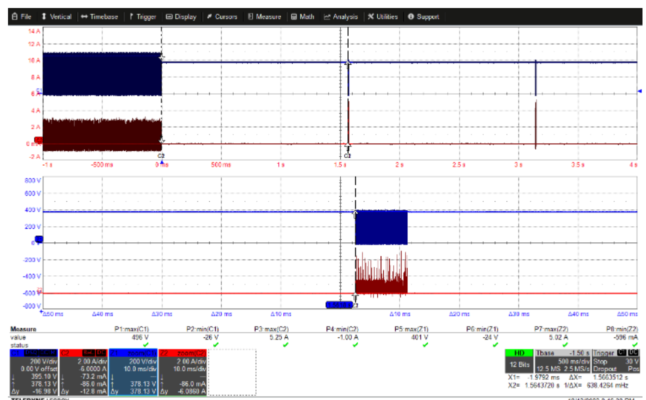


Figure 53 – 265 VAC.
CH1: Drain Voltage: 200 V / div., 500 ms / div.
CH2: Drain Current: 2 A / div., 500 ms / div.
Zoom: 10 ms / div.
Drain Voltage, Max = 496 V.
Drain Current, Max = 5.25 A.

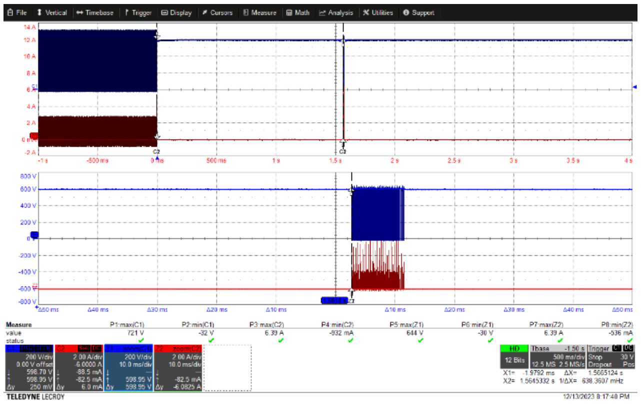


Figure 54 – 420 VAC.
CH 1: Drain Voltage: 200 V / div., 500 ms / div.
CH 2: Drain Current: 2 A / div., 500 ms / div.
Zoom: 10 ms / div.
Drain Voltage, Max = 721 V.
Drain Current, Max = 6.39 A.

11.4 SR FET Switching Waveforms

11.4.1 SR FET Voltage and Current at Start-up

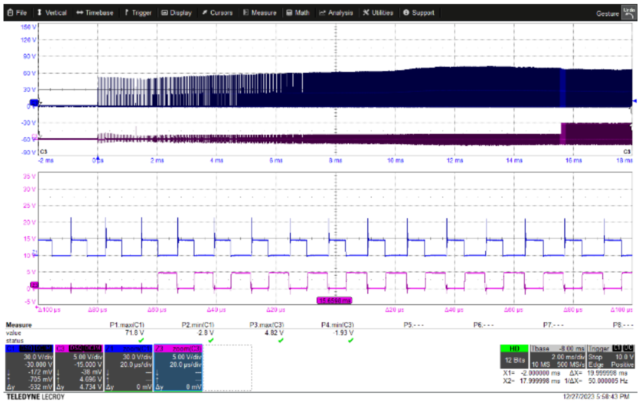


Figure 55 – 90 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 30 V / div., 2 ms / div.
CH 3: Gate Voltage: 5 V / div., 2 ms / div.
Zoom: 20 µs.
SR FET Drain Voltage, Max. = 71.8 V.

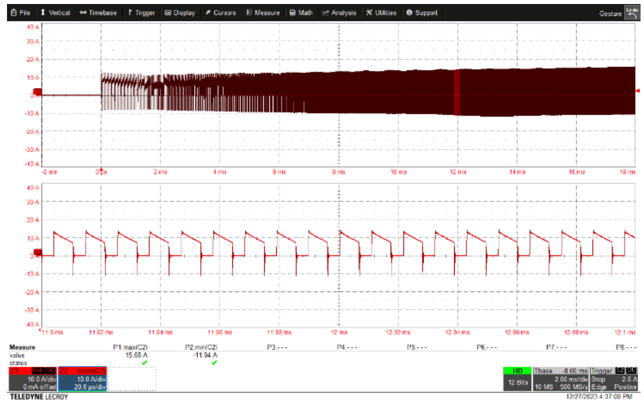


Figure 56 – 90 VAC, I_{OUT} = 5 A (Full-Load).
CH 2: Drain Current: 10 A / div., 2 ms / div.
Zoom: 20 µs.
SR FET Drain Current, Max. = 15.68 A.

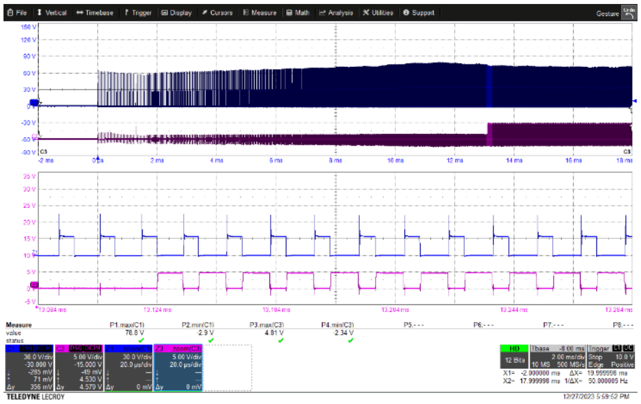


Figure 57 – 115 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 30 V / div., 2 ms / div.
CH 3: Gate Voltage: 5 V / div., 2 ms / div.
Zoom: 20 µs.
SR FET Drain Voltage, Max. = 78.8 V.

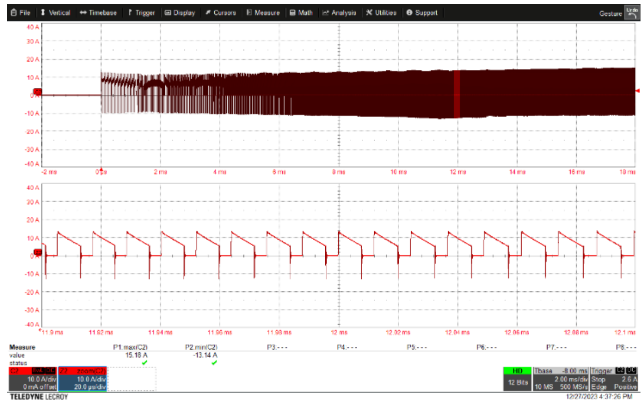


Figure 58 – 115 VAC, I_{OUT} = 5 A (Full-Load).
CH 2: Drain Current: 10 A / div., 2 ms / div.
Zoom: 20 µs.
SR FET Drain Current, Max. = 15.18 A.

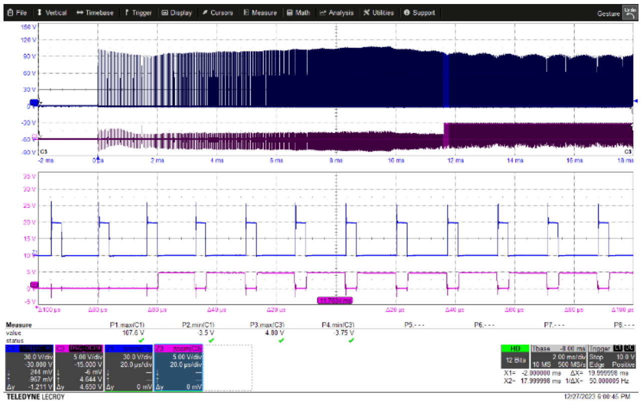


Figure 59 – 230 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 30 V / div., 2 ms / div.
CH 3: Gate Voltage: 5 V / div., 2 ms / div.
Zoom: 20 μs.
SR FET Drain Voltage, Max. = 107.6 V.

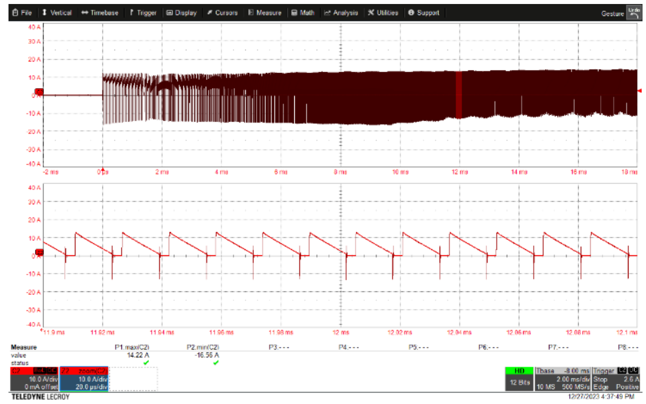


Figure 60 – 230 VAC, I_{OUT} = 5 A (Full-Load).
CH 2: Drain Current: 10 A / div., 2 ms / div.
Zoom: 20 μs.
SR FET Drain Current, Max. = 14.22 A.

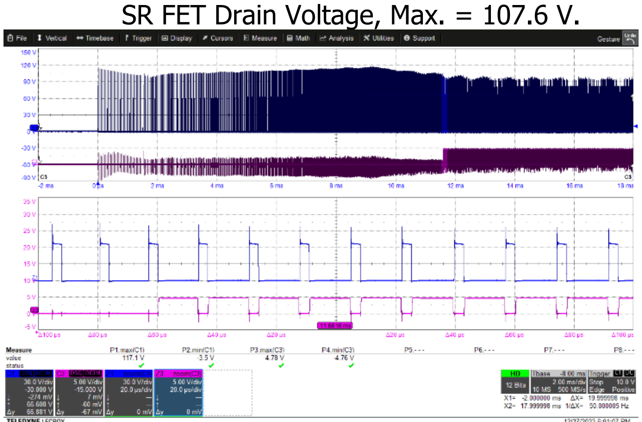


Figure 61 – 265 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 30 V / div., 2 ms / div.
CH 3: Gate Voltage: 5 V / div., 2 ms / div.
Zoom: 20 μs.
SR FET Drain Voltage, Max. = 117.1 V.

Figure 62 – 265 VAC, I_{OUT} = 5 A (Full-Load).
CH 2: Drain Current: 10 A / div., 2 ms / div.
Zoom: 20 μs.
SR FET Drain Current, Max. = 14.14 A.

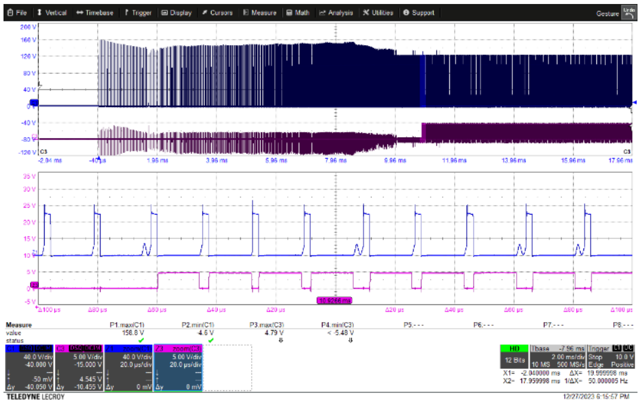


Figure 63 – 420 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 30 V / div., 2 ms / div.
CH 3: Gate Voltage: 5 V / div., 2 ms / div.
Zoom: 20 μs.
SR FET Drain Voltage, Max. = 158.8 V.

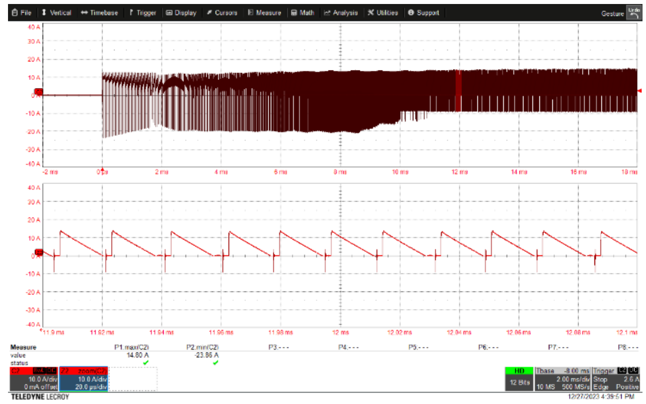


Figure 64 – 420 VAC, I_{OUT} = 5 A (Full-Load).
CH 2: Drain Current: 10 A / div., 2 ms / div.
Zoom: 20 μs.
SR FET Drain Current, Max. = 14.80 A.

11.4.2 SR FET Voltage and Current at Normal Operations

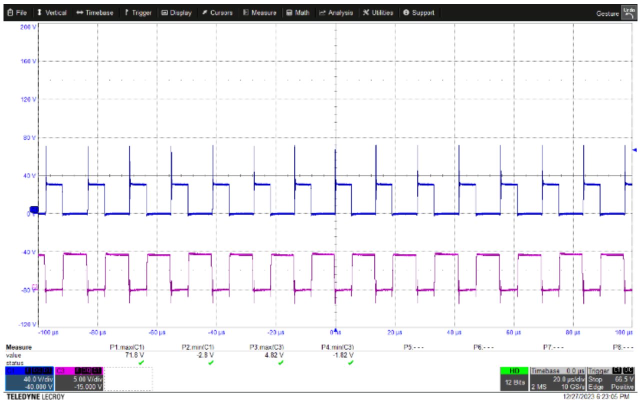


Figure 65 – 90 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 30 V / div., 20 µs / div.
CH 3: Gate Voltage: 5 V / div., 20 µs / div.
SR FET Drain Voltage, Max. = 71.8 V..

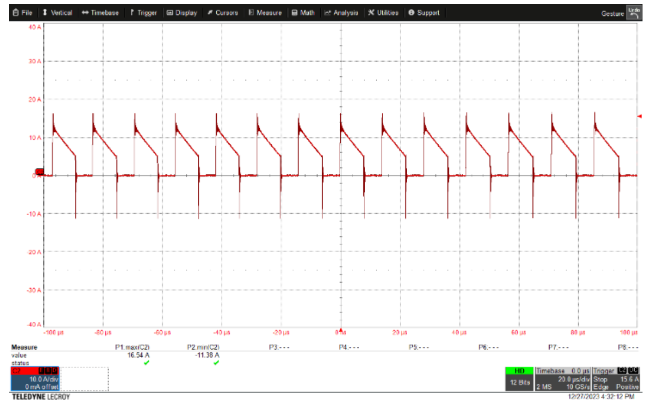


Figure 66 – 90 VAC, I_{OUT} = 5 A (Full-Load).
CH 2: Drain Current: 10 A / div., 20 µs / div.
SR FET Drain Current, Max. = 16.54 A.

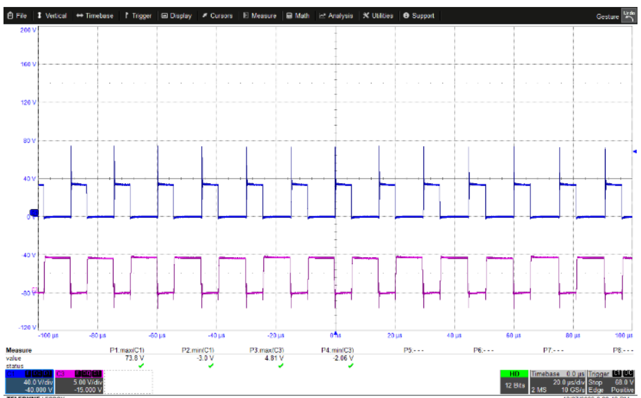


Figure 67 – 115 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 30 V / div., 20 µs / div.
CH 3: Gate Voltage: 5 V / div., 20 µs / div.
SR FET Drain Voltage, Max. = 73.8 V.

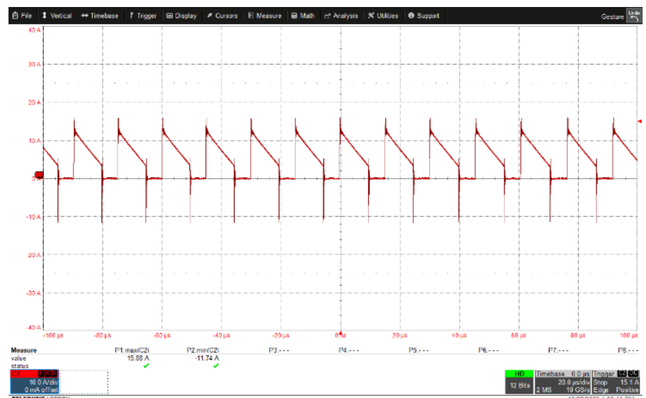


Figure 68 – 115 VAC, I_{OUT} = 5 A (Full-Load).
CH 2: Drain Current: 10 A / div., 20 µs / div.
SR FET Drain Current, Max. = 15.88 A.

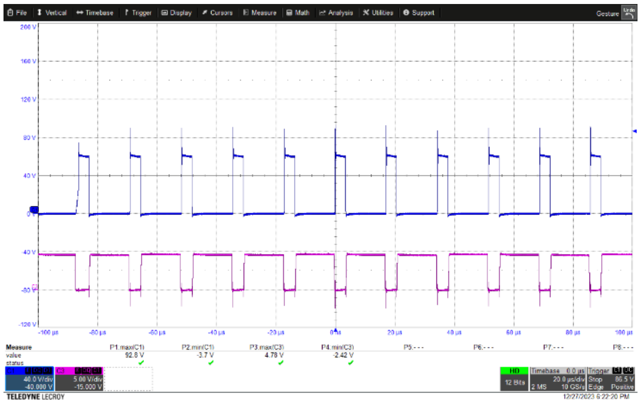


Figure 69 – 230 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 30 V / div., 20 µs / div.
CH 3: Gate Voltage: 5 V / div., 20 µs / div.
SR FET Drain Voltage, Max. = 92.8 V.

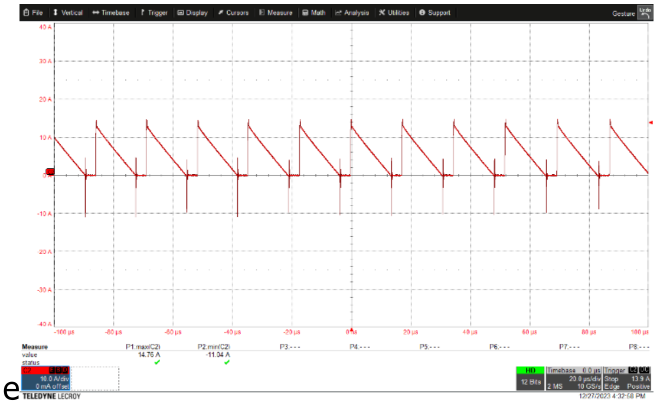


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Figure 70 – 230 VAC, I_{OUT} = 5 A (Full-Load).
CH 2: Drain Current: 10 A / div., 20 µs / div.
SR FET Drain Current, Max. = 14.76 A.

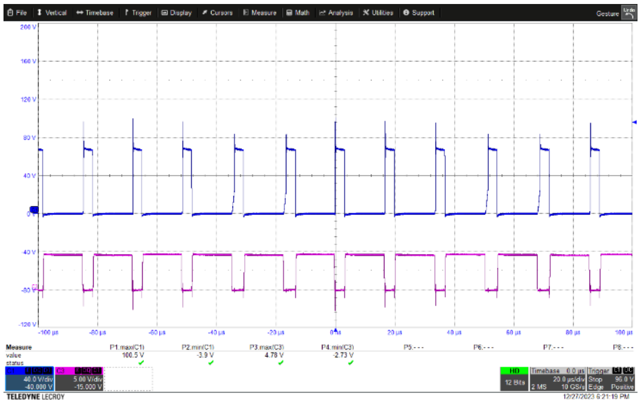

Figure 71 – 265 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 30 V / div., 20 µs / div.
CH 3: Gate Voltage: 5 V / div., 20 µs / div.
SR FET Drain Voltage, Max. = 100.5 V.

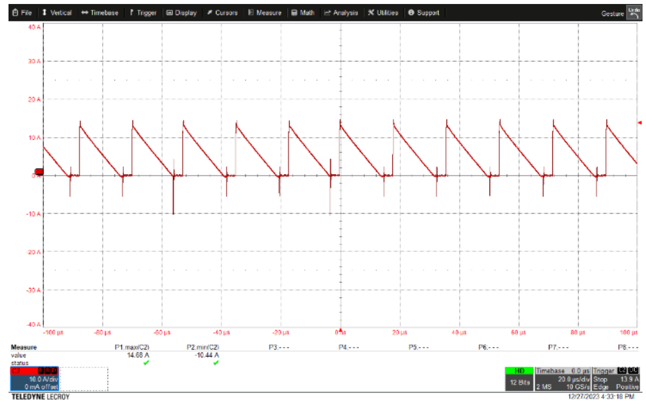

Figure 72 – 265 VAC, I_{OUT} = 5 A (Full-Load).
CH 2: Drain Current: 10 A / div., 20 µs / div.
SR FET Drain Current, Max. = 14.68 A.

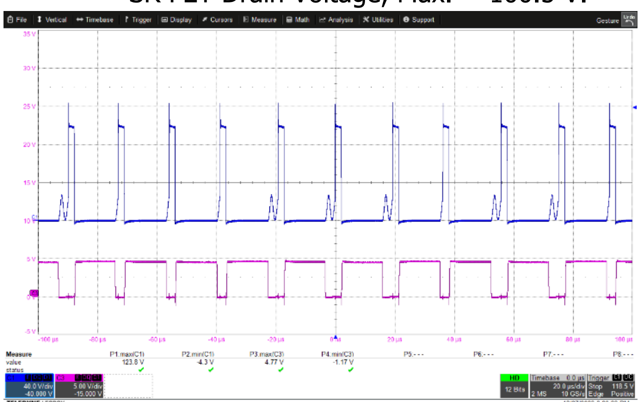

Figure 73 – 420 VAC, I_{OUT} = 5 A (Full-Load).
CH 1: Drain Voltage: 30 V / div., 20 µs / div.
CH 3: Gate Voltage: 5 V / div., 20 µs / div.
SR FET Drain Voltage, Max. = 123.8 V.

e

Figure 74 – 420 VAC, I_{OUT} = 5 A (Full-Load).
CH 2: Drain Current: 10 A / div., 20 µs / div.
SR FET Drain Current, Max. = 15.04 A.

11.5 Output Ripple Measurements

11.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The PP026 probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

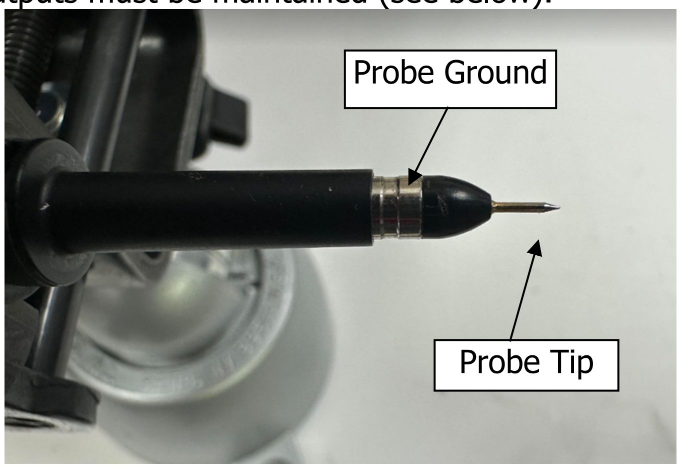

Figure 75 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

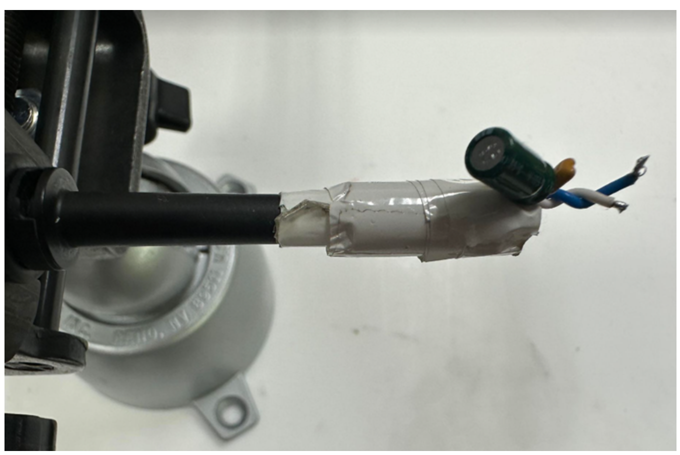

Figure 76 – Oscilloscope Probe with BNC Adapter

(https://www.teledynelecroy.com/probes/passive-probes/pp026-1)

11.5.2 Ripple Waveforms (Measured on Board)

11.5.2.1 100% Load

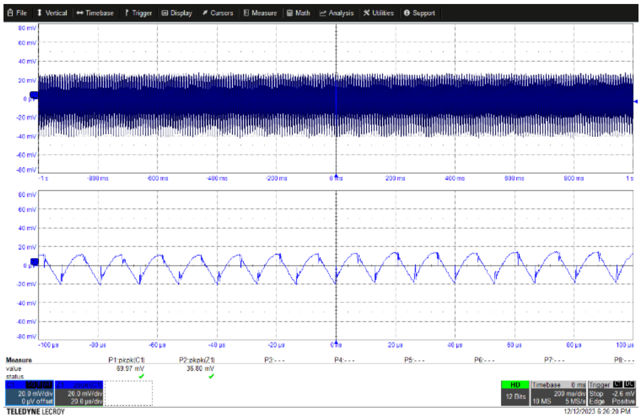

Figure 77 –90 VAC Input, 100% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 69.97 mV_{PP}.

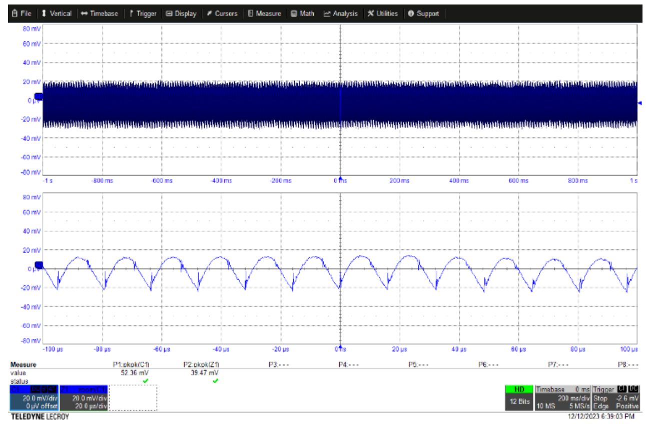

Figure 78 – 115 VAC Input, 100% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 52.36 mV_{PP}.

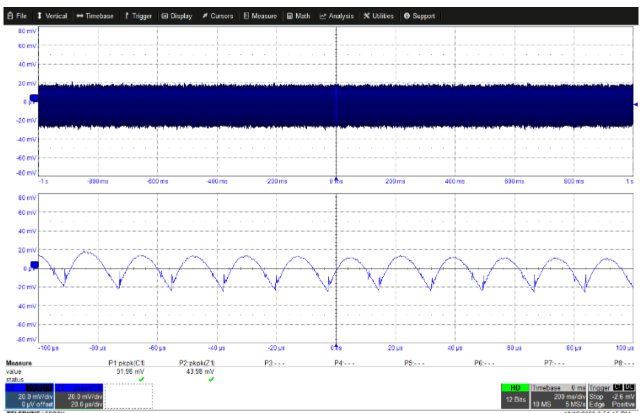

Figure 79 – 230 VAC Input, 100% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 51.98 mV_{PP}.

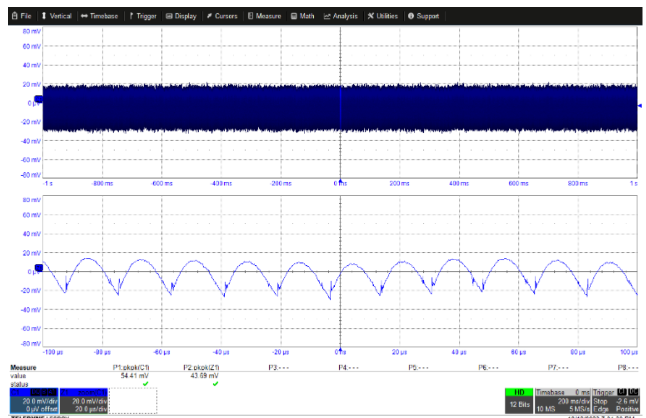

Figure 80 – 265 VAC Input, 100% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 54.41 mV_{PP}.

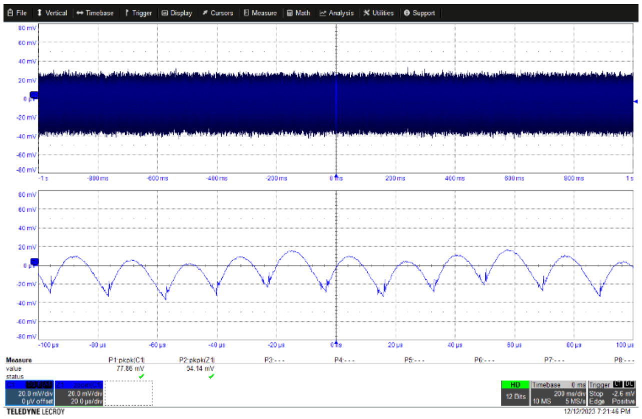

Figure 81 – 420 VAC Input, 100% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 77.86 mV_{PP}.

11.5.2.2 50% Load

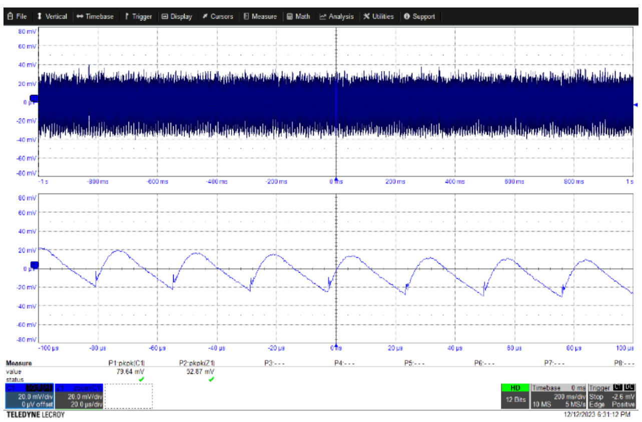

Figure 82 –90 VAC Input, 50% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 79.64 mV_{PP}.

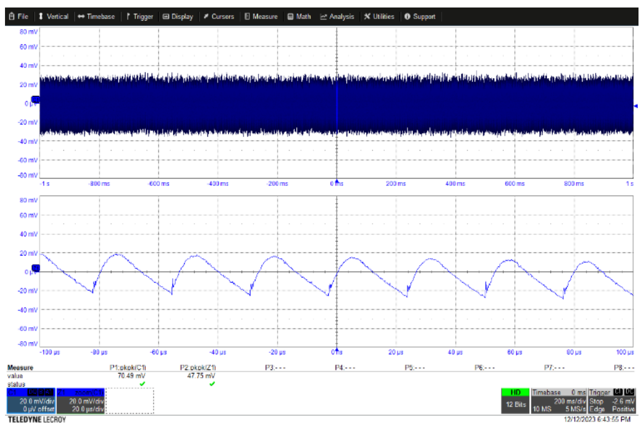

Figure 83 – 115 VAC Input, 50% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 70.49 mV_{PP}.

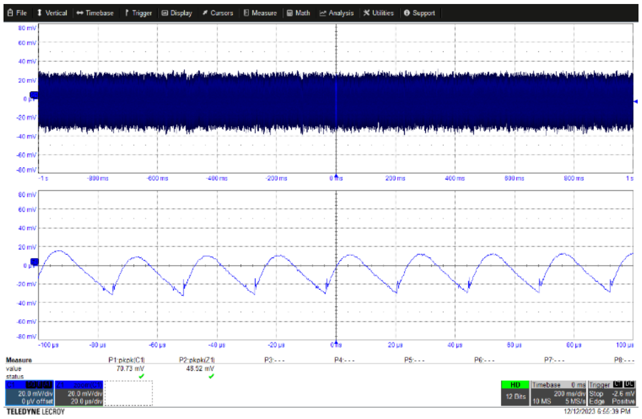

Figure 84 – 230 VAC Input, 50% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 70.73 mV_{PP}.

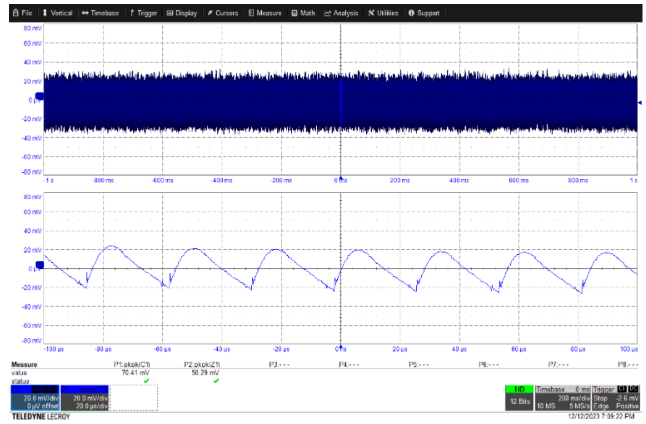

Figure 85 – 265 VAC Input, 50% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 70.41 mV_{PP}.

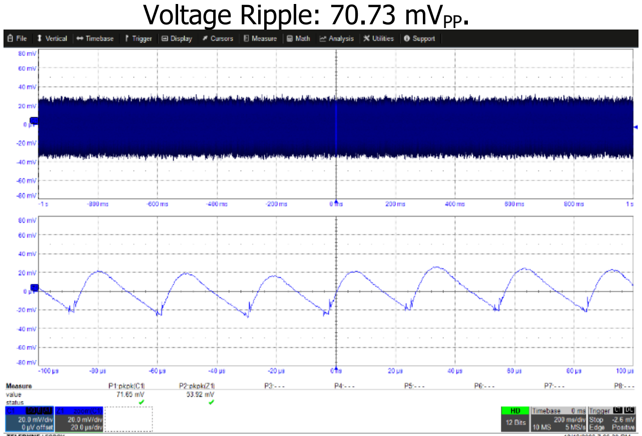

Figure 86 – 420 VAC Input, 50% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 71.65 mV_{PP}.

11.5.2.3 10% Load

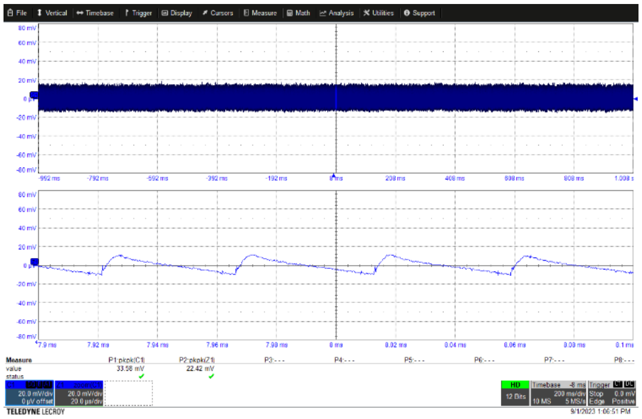

Figure 87 – 90 VAC Input, 10% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 33.58 mV_{PP}.

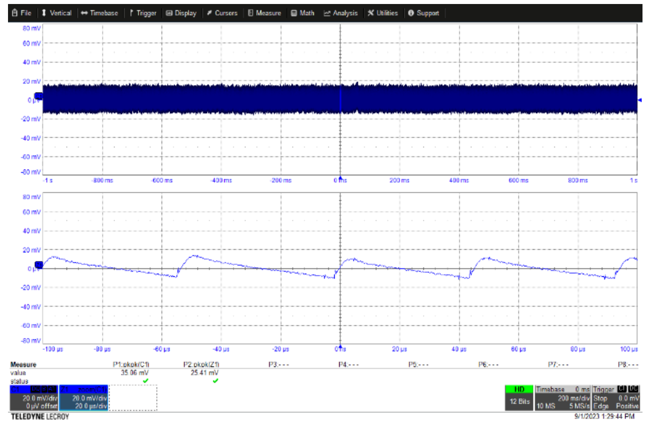

Figure 88 – 115 VAC Input, 10% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 35.06 mV_{PP}.

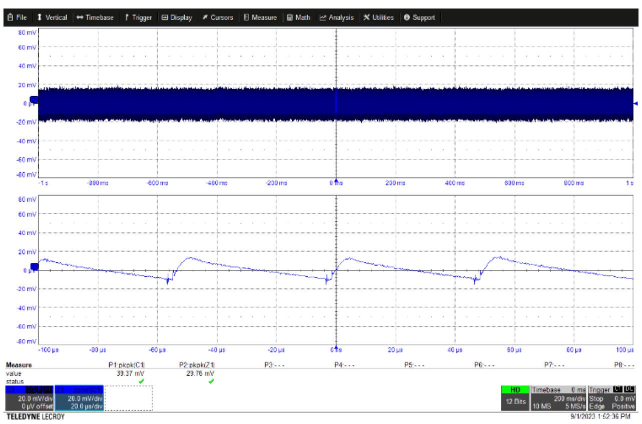

Figure 89 – 230 VAC Input, 10% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 39.37 mV_{PP}.

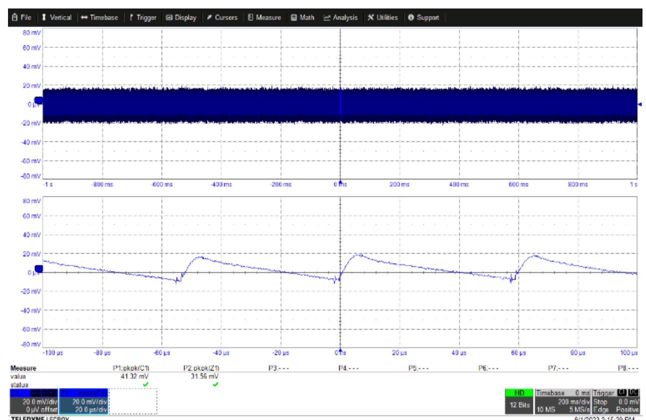

Figure 90 – 265 VAC Input, 10% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 41.32 mV_{PP}.

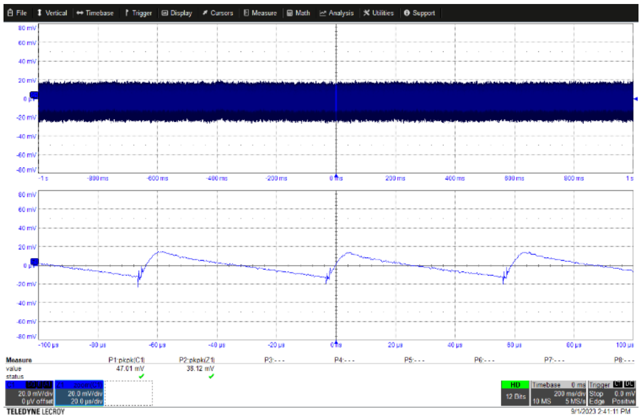

Figure 91 – 420 VAC Input, 10% Load.
V_{OUT}, 20 mV / div., 200 ms / div.
Zoom: 20 µs.
Voltage Ripple: 47.01 mV_{PP}.

11.5.3 Output Voltage Ripple

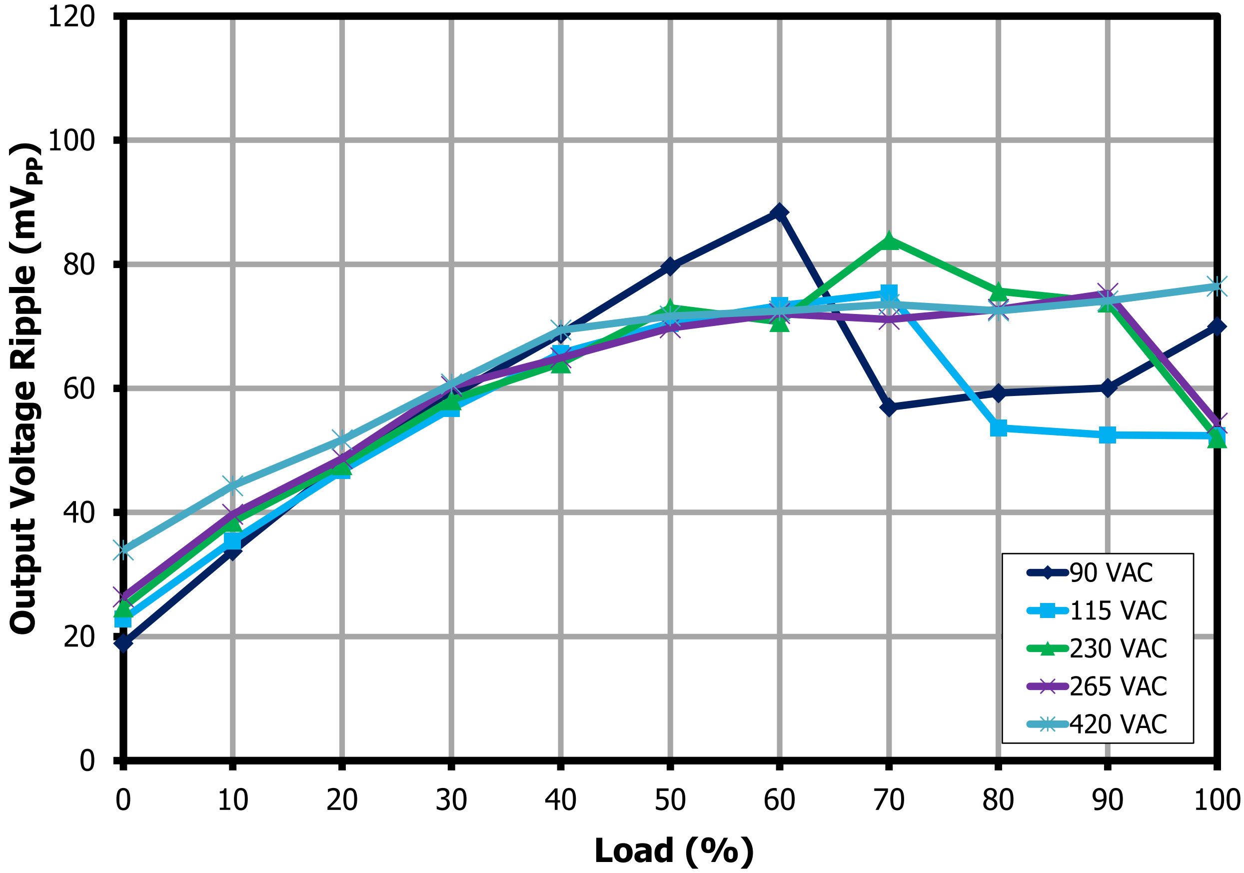

Figure 92 – Output Voltage Ripple**.**

11.6 Input Undervoltage and Overvoltage Detection

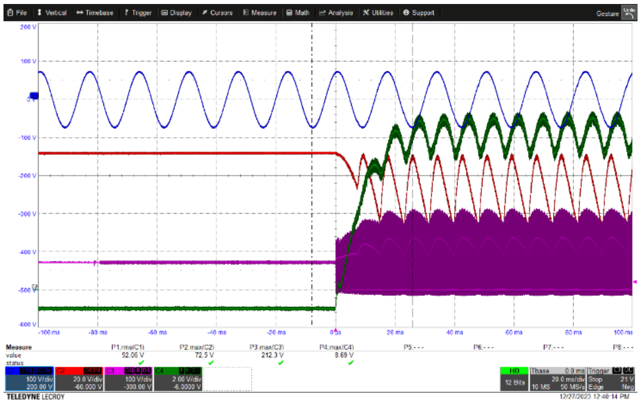

Figure 93 – UV+, I_{OUT} = 5 A (Full-Load).
CH 1: Input Voltage: 100 V / div., 20 ms / div.
CH 2: Bulk Voltage: 20 V / div., 20 ms / div.
CH 3: VDS (InnoSwitch): 100 V / div., 20 ms / div.
CH 4: Output Voltage: 2 V / div., 20 ms / div.
UV+ = 52.06 V_{RMS}.

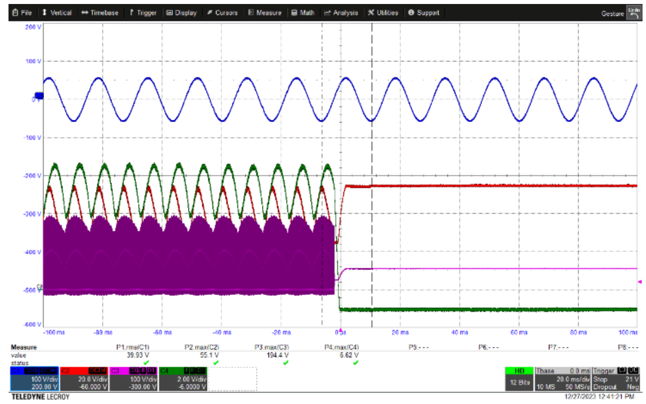

Figure 94 – UV-, I_{OUT} = 5 A (Full-Load).
CH 1: Input Voltage: 100 V / div., 20 ms / div.
CH 2: Bulk Voltage: 20 V / div., 20 ms / div.
CH 3: VDS (InnoSwitch): 100 V / div., 20 ms / div.
CH 4: Output Voltage: 2 V / div., 20 ms / div.
UV- = 39.93 V_{RMS}.

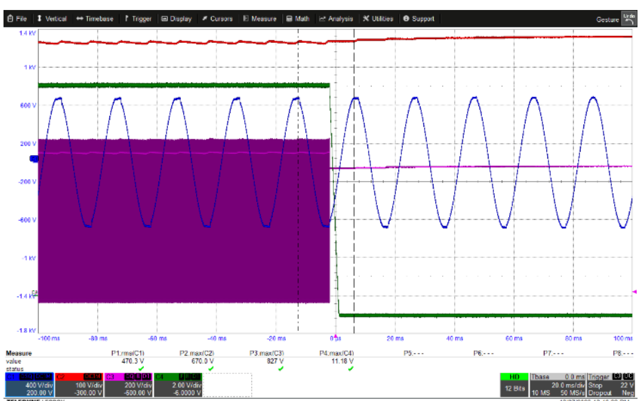

Figure 95 – OV+, I_{OUT} = 5 A (Full-Load).
CH 1: Input Voltage: 100 V / div., 20 ms / div.
CH 2: Bulk Voltage: 20 V / div., 20 ms / div.
CH 3: VDS (InnoSwitch): 100 V / div., 20 ms / div.
CH 4: Output Voltage: 2 V / div., 20 ms / div.
OV+ = 470.3 V_{RMS}.

12 Conducted EMI

12.1 Grounded Output

12.1.1 VIN: 115 VAC

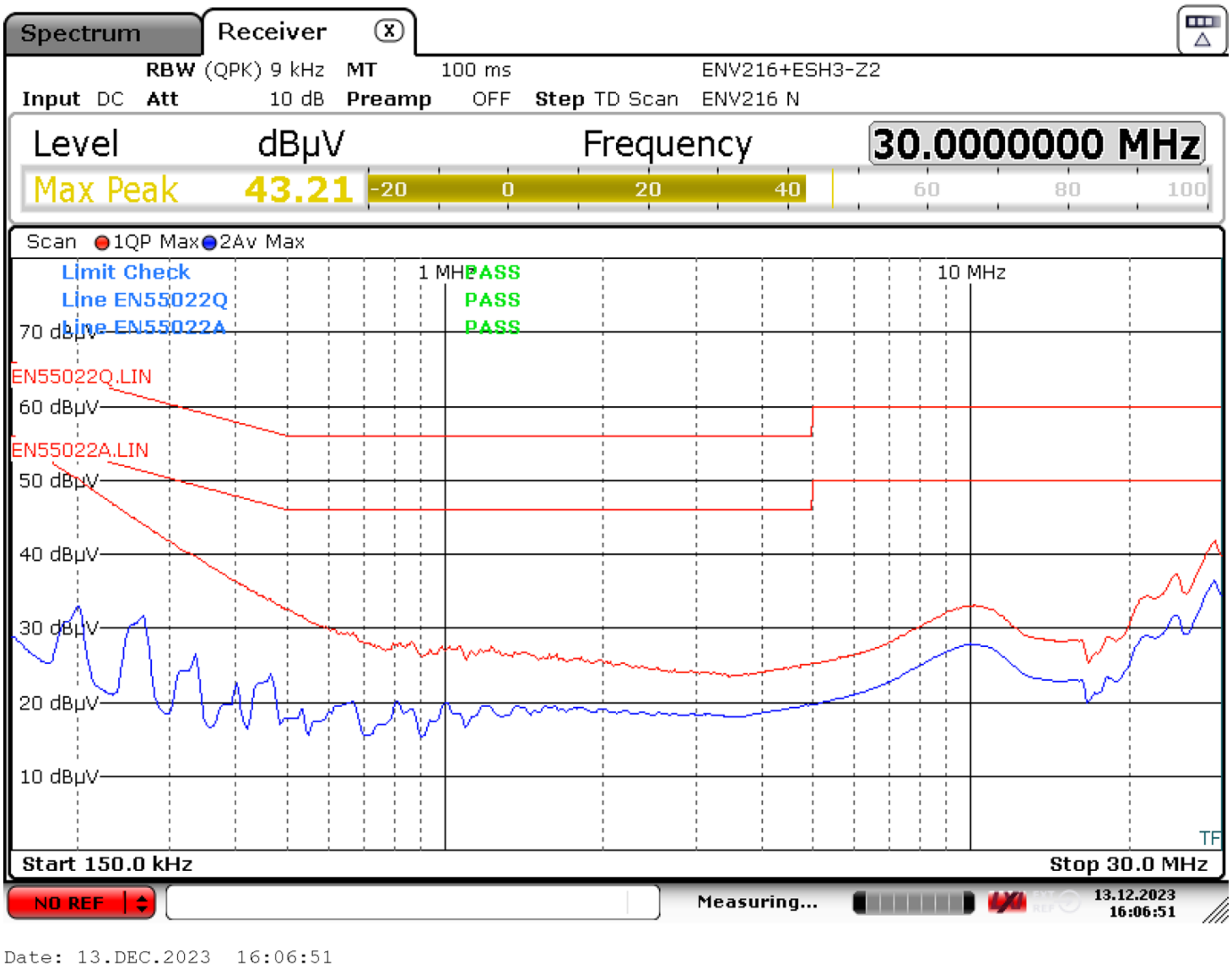

Figure 96 – Grounded Output EMI, Line, 12 V / 100% Load.

12.1.2 VIN: 230 VAC

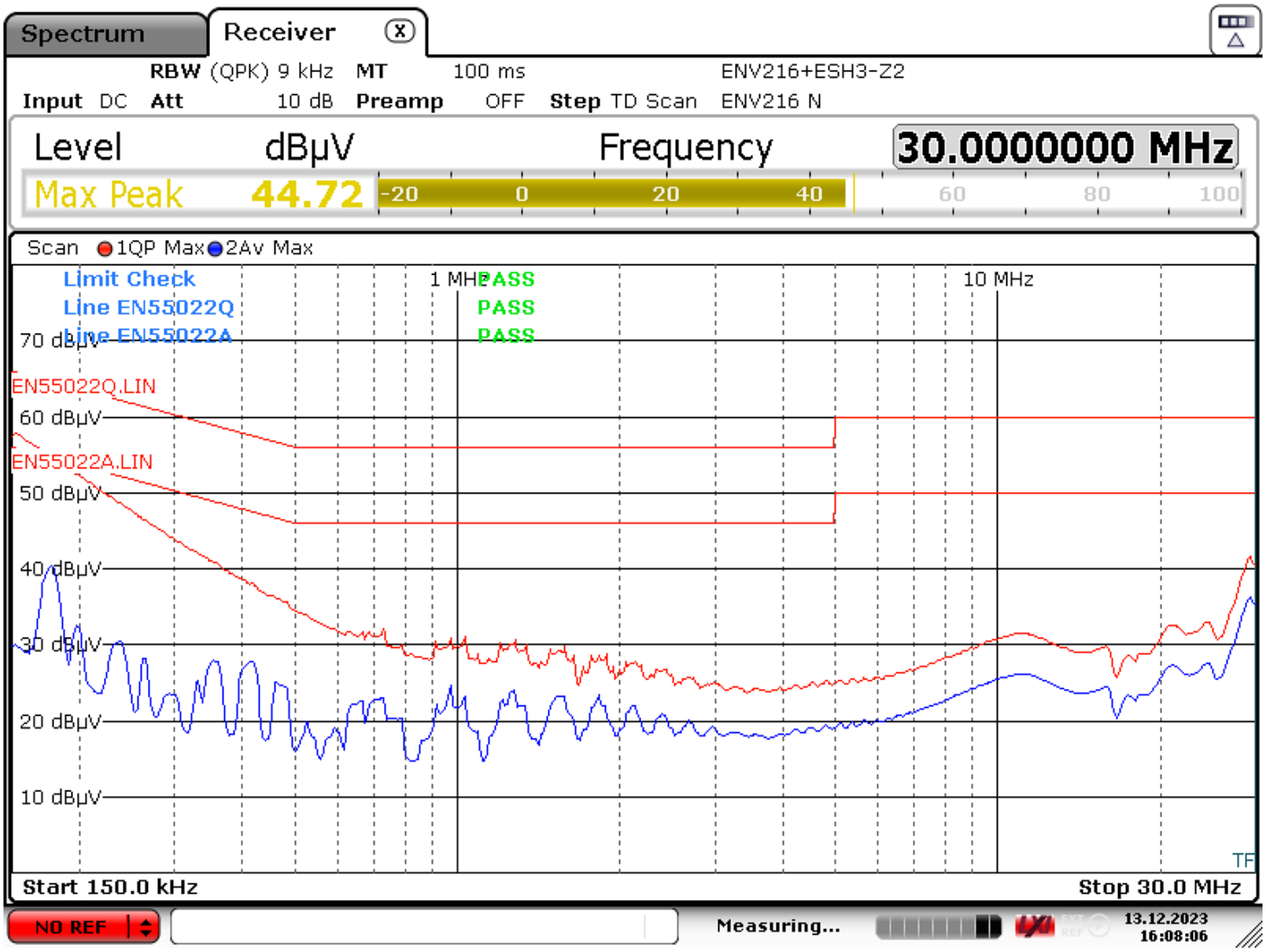

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Figure 97 – Grounded Output EMI, Line, 12 V / 100% Load.

13 Line Surge

13.1 Differential Mode Test

Surge Voltage (V)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+6000	90	L, N	2	10	Pass
–6000	90	L, N	2	10	Pass
+6000	180	L, N	2	10	Pass
–6000	180	L, N	2	10	Pass
+6000	270	L, N	2	10	Pass
–6000	270	L, N	2	10	Pass

13.2 Ring Wave Surge

Surge Voltage (V)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+6000	90	L, N → PE	12	10	Pass
–6000	90	L, N → PE	12	10	Pass
+6000	180	L, N → PE	12	10	Pass
–6000	180	L, N → PE	12	10	Pass
+6000	270	L, N → PE	12	10	Pass
–6000	270	L, N → PE	12	10	Pass

14 EFT

Surge Voltage (V)	Phase Angle (º)	IEC Coupling	Frequency (kHz)	Burst Time	Reception Time (ms)	Step Duration (s)	Result
+4000	90	L, N - PE	5	15 ms	300	120	Pass
–4000	90	L, N - PE	5	15 ms	300	120	Pass
+4000	180	L, N - PE	5	15 ms	300	120	Pass
–4000	180	L, N - PE	5	15 ms	300	120	Pass
+4000	270	L, N - PE	5	15 ms	300	120	Pass
–4000	270	L, N - PE	5	15 ms	300	120	Pass
+4000	90	L, N - PE	100	750 μs	300	120	Pass
–4000	90	L, N - PE	100	750 μs	300	120	Pass
+4000	180	L, N - PE	100	750 μs	300	120	Pass
–4000	180	L, N - PE	100	750 μs	300	120	Pass
+4000	270	L, N - PE	100	750 μs	300	120	Pass
–4000	270	L, N - PE	100	750 μs	300	120	Pass

15 ESD

Passed ±16.5 kV air discharge and ±8.8 kV contact discharge at both output positive and negative terminals, under full-load condition for both 115 VAC and 230 VAC.

15.1 Contact Discharge at 115 VAC and 230 VAC

Contact Discharge (kV)	Point of Discharge	Number of Strikes	No. of Auto-Restart	Test Result
+ 2	V_{OUT} (+)	10	0/10	PASS
- 2		10	0/10	PASS
+ 2	V_{OUT} (-)	10	0/10	PASS
- 2		10	0/10	PASS
+ 4	V_{OUT} (+)	10	0/10	PASS
- 4		10	0/10	PASS
+ 4	V_{OUT} (-)	10	0/10	PASS
- 4		10	0/10	PASS
+ 6	V_{OUT} (+)	10	0/10	PASS
- 6		10	0/10	PASS
+ 6	V_{OUT} (-)	10	0/10	PASS
- 6		10	0/10	PASS
+ 8	V_{OUT} (+)	10	0/10	PASS
- 8		10	0/10	PASS
+ 8	V_{OUT} (-)	10	0/10	PASS
- 8		10	0/10	PASS
+ 8.8	V_{OUT} (+)	10	0/10	PASS
- 8.8		10	0/10	PASS
+ 8.8	V_{OUT} (-)	10	0/10	PASS
- 8.8		10	0/10	PASS

15.2 Air Discharge at 115 VAC and 230 VAC

Air Discharge (kV)	Point of Discharge	Number of Strikes	No. of Auto-Restart	Test Result
+ 8	V_{OUT} (+)	10	0/10	PASS
- 8		10	0/10	PASS
+ 8	V_{OUT} (-)	10	0/10	PASS
- 8		10	0/10	PASS
+ 10	V_{OUT} (+)	10	0/10	PASS
- 10		10	0/10	PASS
+ 10	V_{OUT} (-)	10	0/10	PASS
- 10		10	0/10	PASS
+ 12	V_{OUT} (+)	10	0/10	PASS
- 12		10	0/10	PASS
+ 12	V_{OUT} (-)	10	0/10	PASS
- 12		10	0/10	PASS
+ 14	V_{OUT} (+)	10	0/10	PASS
- 14		10	0/10	PASS
+ 14	V_{OUT} (-)	10	0/10	PASS
- 14		10	0/10	PASS
+ 15	V_{OUT} (+)	10	0/10	PASS
- 15		10	0/10	PASS
+ 15	V_{OUT} (-)	10	0/10	PASS
- 15		10	0/10	PASS
+ 16.5	V_{OUT} (+)	10	0/10	PASS
- 16.5		10	0/10	PASS
+ 16.5	V_{OUT} (-)	10	0/10	PASS
- 16.5		10	0/10	PASS

16 Revision History

Date	Author	Revision	Description & Changes	Reviewed
10-Apr-24	JMR	1.0	Initial Release	Apps & Mktg

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